Design of Reversible/Quantum Ternary Multiplexer and Demultiplexer

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Abstract: In this paper, we show realization of macro-level ternary reversible 2-qudit Feynman gate, 3-qudit controlled Feynman gate, and 3-qudit Toffoli gates using ternary reversible 1-qudit gates and 2-qudit Muthukrishnan-Stroud gates, which are theoretically realizable using quantum technology such as liquid ion trap [10]. Then we show the design of ternary reversible multiplexer and demultiplexer using the macro-level gates.

Keywords: Demultiplexer, logic synthesis, multiplexer, quantum circuits, reversible circuits, ternary logic.

1. Introduction

Ternary reversible/quantum logic synthesis is a new and immature research area [1-9]. Papers [4, 7] presented ternary quantum logic synthesis methods using 2-qudit (*qu*antum *dig*it) Generalized Ternary Gate (GTG) family [1], which is a macro-level gate family and is needed to be realized using primitive quantum gates. Papers [2, 3, 5, 6] presented ternary quantum logic synthesis methods using multi-qudit macro-level gates, which are also needed to be realized using primitive quantum gates. Papers [1-7] presented generalized synthesis techniques but did not give synthesis examples of practically important ternary circuits like adder, subtractor, encoder, decoder, multiplexer, demultiplexer, etc., except the synthesis of ternary adder circuits in [4, 5]. These circuits are major sub-circuits needed for digital system design. Synthesis of ternary reversible/quantum adder/subtractor is given in [8] and realization of ternary reversible/quantum encoder and decoder is given in [9]. In this paper we present design of reversible/quantum realization of ternary multiplexer and demultiplexer circuits. For this purpose, we show realization of macro-level ternary reversible 2-qudit Feynman gate, 3-qudit controlled Feynman gate, and 3-qudit Toffoli gates using ternary reversible 1-qudit gates and 2-qudit Muthukrishnan-Stroud gates, which are theoretically realizable using quantum technology such as liquid ion trap [10]. Then we show the design of ternary reversible multiplexer and demultiplexer using the macro-level gates.

2. Ternary 1-qudit permutative gates

Any transformation of the qudit state represented by a 3×3 unitary matrix specifies a valid 1-qudit ternary quantum gate. There are many such non-trivial 1-qudit gates. However, in this work, we use only the unitary permutative transforms as shown by permutative matrices of Figure 1. Transforms $Z(+1)$ and $Z(+2)$ shift the qudit states by 1 and 2, respectively. Transform $Z(12)$ permutes the qudit states $|1\rangle$ and $|2\rangle$, $Z(01)$ permutes the qudit states $|0\rangle$ and $|1\rangle$, and $Z(02)$ permutes the qudit states $|0\rangle$ and $|2\rangle$ without affecting the other qudit state. The input-output relationships of these 1-qudit gates are shown in truth table form in Table 1. The ternary reversible 1-qudit gates are elementary gates and can be theoretically realized using quantum technology such as liquid ion trap technology [10]. Therefore, we assign them a cost of 1.

$$Z(+1)=\begin{bmatrix}0&0&1\\1&0&0\\0&1&0\end{bmatrix}\quad Z(+2)=\begin{bmatrix}0&1&0\\0&0&1\\1&0&0\end{bmatrix}$$

$$Z(12)=\begin{bmatrix}1&0&0\\0&0&1\\0&1&0\end{bmatrix}\quad Z(01)=\begin{bmatrix}0&1&0\\1&0&0\\0&0&1\end{bmatrix}$$

$$Z(02)=\begin{bmatrix}0&0&1\\0&1&0\\1&0&0\end{bmatrix}$$

Figure 1. 1-qudit ternary unitary permutative transforms.

Table 1. Truth table of 1-qudit ternary reversible gates.

Input	Output				
	+1	+2	12	01	02
0	1	2	0	1	2
1	2	0	2	0	1
2	0	1	1	2	0

If two 1-qudit gates x and y in cascade have the resultant effect that the input signal to the gate x is restored at the output of the gate y, then the gate y is said to be the *inverse gate* of the gate x. Table 2 shows the inverse gates of all the 1-qudit gates.

Table 2. 1-qudit ternary reversible gates and their inverse gates.

Gate	$Z(+1)$	$Z(+2)$	$Z(12)$	$Z(01)$	$Z(02)$
Inverse gate	$Z(+2)$	$Z(+1)$	$Z(12)$	$Z(01)$	$Z(02)$

3. Ternary Muthukrishnan-Stroud gates

Muthukrishnan and Stroud [10] proposed a family of 2-qudit d-valued gates, which applies a 1-qudit unitary transform on the second qudit conditional on the first qudit being (d – 1). Figure 1 and Table 1 show five such ternary (d = 3) unitary permutative transforms and Figure 2 gives the symbolic representation of ternary Muthukrishnan-Stroud (M-S) gates. The ternary M-S gates can be theoretically realized using quantum technology such as liquid ion trap technology as an elementary gate [10]. Therefore, we assign these gates a cost of 1.

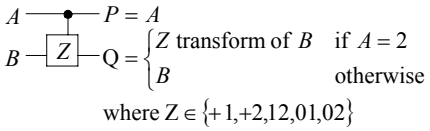
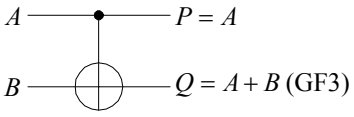


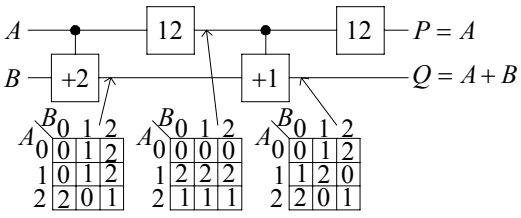
Figure 2. Symbol of 2-qudit ternary Muthukrishnan-Stroud gates [cost = 1].

4. Ternary Feynman gates

We propose ternary counter part of binary Feynman gate in Figure 3(a), where the output $P = A$ and the output $Q = A + B$ (GF3). The realization of the gate using M-S gates is shown in Figure 3(b). The second 12 gate along the input line A is the inverse gate of the first 12 gate, which restores the input signal A. The truth tables along the input line B verify that the output $Q = A + B$ (GF3). The cost of the realization is 4.



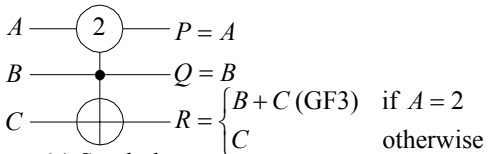
(a) Symbol



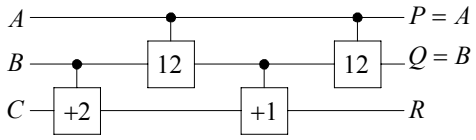
(b) Realization using M-S gates

Figure 3. 2-qudit ternary Feynman gate [cost=4].

We propose a 3-qudit controlled Feynman gate as shown in Figure 4(a). The outputs are $P = A$, $Q = B$, and $R = B + C$ (GF3) if $A = 2$, otherwise $R = C$. The realization of the gate using M-S gates is shown in Figure 4(b). The output P is always equal to A. When $A = 2$, then the 12 gates along the input line B will be active and the circuit will become equivalent to the circuit of Figure 3(b) and the outputs will be $Q = B$ and $R = B + C$ (GF3). If $A \neq 2$, then the 12 gates along the input line B will not be active and the output Q will be equal to B. In this situation, if $B \neq 2$, then the +2 and +1 gates along the input line C will not be active and the output R will be equal to C. But, if $B = 2$, then the +2 and +1 gates along the input line C will be active, but as +1 gate is the inverse gate of +2 gate, there will be no change of input C and the output R will be equal to C. The cost of the realization is 4.



(a) Symbol

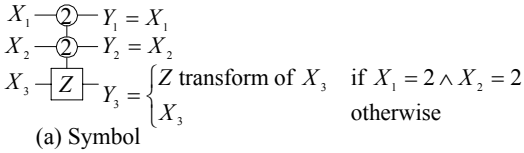


(b) Realization using M-S gates

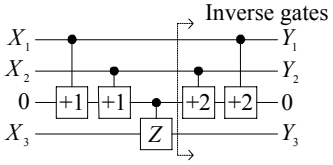
Figure 4. 3-qudit ternary controlled Feynman gate [cost=4].

5. Ternary Toffoli gates

We propose a 3-qudit ternary Toffolli gate as shown in Figure 5(a), where X_1 and X_2 are two controlling inputs and X_3 is the controlled input. If the two controlling input values are 2, then Z transform is applied on the controlled input, otherwise the controlled input is passed unchanged. Realization of this gate using M-S gates is shown in Figure 5(b), where a constant input 0 is changed to 2 by using two +1 transforms controlled from the two controlling inputs X_1 and X_2, and then the resultant constant 2 is used to control the input X_3. The right most two gates are the inverse gates of the left most two gates used to restore the constant input 0. The cost of this realization is 5.



(a) Symbol



(b) Realization using M-S gates

Figure 5. 3-qudit ternary Toffoli gate [cost=5].

6. Ternary Reversible Decoder with Active-2 Outputs

We will use ternary reversible decoder with active-2 outputs for designing both ternary reversible multiplexer and demultiplexer. The design of ternary reversible decoders is discussed in [9]. The truth table of a 2×9 ternary decoder with active-2 output is shown in Table 3. For a given input combination, only the selected output will be 2 and the remaining outputs will be 0. Realization of the ternary reversible decoder is shown in Figure 6 adopted from [9]. The cost of this realization is 5×9+12=57.

Table 3. Truth table of a 2×9 ternary decoder with active-2 output

A_1	A_0	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	2
0	1	0	0	0	0	0	0	0	2	0
0	2	0	0	0	0	0	0	2	0	0
1	0	0	0	0	0	0	2	0	0	0
1	1	0	0	0	0	2	0	0	0	0
1	2	0	0	0	2	0	0	0	0	0
2	0	0	0	2	0	0	0	0	0	0
2	1	0	2	0	0	0	0	0	0	0
2	2	2	0	0	0	0	0	0	0	0

7. Realization of Ternary Reversible Multiplexer

The truth table of a 9×1 ternary multiplexer is shown in Table 4, where the output is equal to the selected input. The realization of the multiplexer is shown in Figure 7. Depending on the select combination, one of the decoder outputs becomes 2 and the other decoder outputs remain 0. The 0-outputs do not drive the corresponding controlled Feynman gates. The 2-output drives the corresponding controlled Feynman gate and the multiplexer output becomes exactly equal to the corresponding multiplexer input. For example, if $A_0 = 0$ and $A_1 = 0$, then the decoder output O_0 becomes 2 and the remaining decoder outputs become 0. In this situation, only the first controlled Feynman gate from the left will be active and the multiplexer output will be equal to I_0. The cost of the realization is 102.

8. Realization of Ternary Reversible Demultiplexer

The truth table of a 1×9 ternary demultiplexer is shown in Table 5, where only the selected output is equal to the input I and the remaining outputs are 0. The realization of the demultiplexer is shown in Figure 8. Depending on the select combination, one of the decoder outputs becomes 2 and the other outputs remain 0. The 0-outputs do not drive the corresponding controlled Feynman gates. The 2-output drives the corresponding controlled Feynman gate and the corresponding demultiplexer output becomes exactly equal to the demultiplexer input. For example, if $A_0 = 0$ and $A_1 = 0$, then the decoder output O_0 becomes 2 and the remaining decoder outputs become 0. In this situation, only the first controlled Feynman gate from the left will be active and the demultiplexer output O_0 will be equal to the demultiplexer input I and the other demultiplxer outputs will be 0. The cost of the realization is 102.

Table 4. Truth table of a 9×1 ternary multiplexer.

$A_1 A_0$	Output, O
00	I_0
01	I_1
02	I_2
10	I_3
11	I_4
12	I_5
20	I_6
21	I_7
22	I_8

Table 5. Truth table of a 1×9 ternary demultiplexer.

A_1	A_0	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	I
0	1	0	0	0	0	0	0	0	I	0
0	2	0	0	0	0	0	0	I	0	0
1	0	0	0	0	0	0	I	0	0	0
1	1	0	0	0	0	I	0	0	0	0
1	2	0	0	0	I	0	0	0	0	0
2	0	0	0	I	0	0	0	0	0	0
2	1	0	I	0	0	0	0	0	0	0
2	2	I	0	0	0	0	0	0	0	0

9. Conclusion

In this paper, we propose macro-level ternary reversible 2-qudit Feynman gate and 3-qudit controlled Feynman gate and show their realizations using ternary reversible 1-qudit gates and 2-qudit Muthukrishnan-Stroud gates, which are theoretically realizable using quantum technology such as liquid ion trap technology [10]. We also propose macro-level ternary reversible 3-qudit Toffoli gates and show its realization using ternary reversible 1-qudit and 2-qudit Muthukrishnan-Stroud gates. We also show the realization of a 2×9 ternary reversible decoder with active-2 outputs adopted from [9]. Finally we show realization of a 9×1 ternary reversible multiplexer and a 1×9 ternary reversible demultiplexer. The cost of these realization is 102 each. Using the similar techniques, ternary reversible multiplexers and demultiplexers of any size can be realized.

In our future works, we are planing to realize ternary reversible circuits for incrementer, decrementer, normal ternary to ternary Gray code converter, ternary Gray code

to normal ternary code converter, any code to other code converters, etc.

10. References

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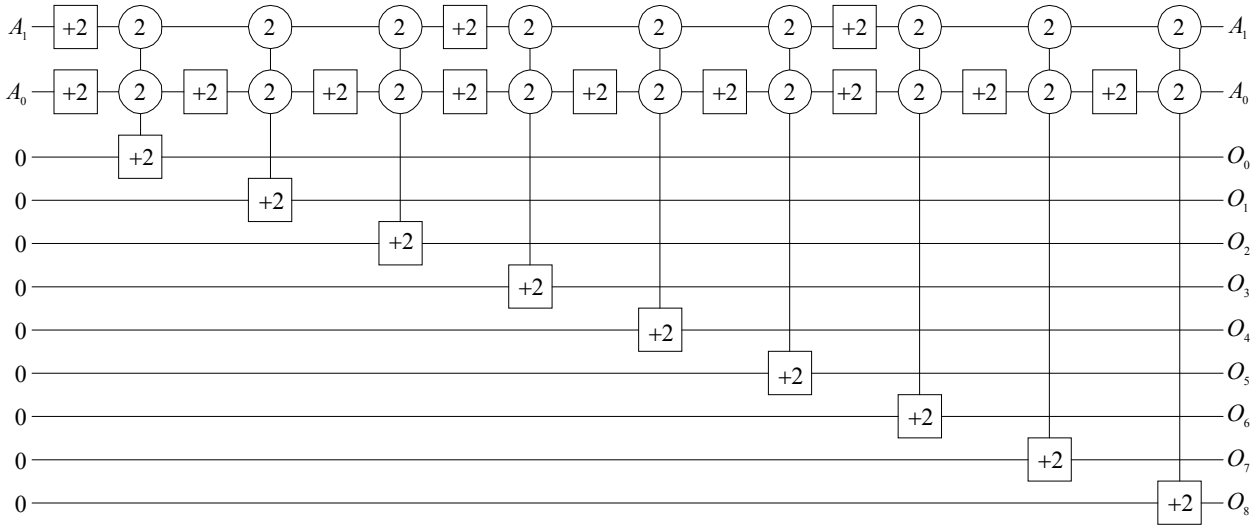

Figure 6. Realization of a 2×9 ternary reversible decoder with active-2 outputs [cost = 57].

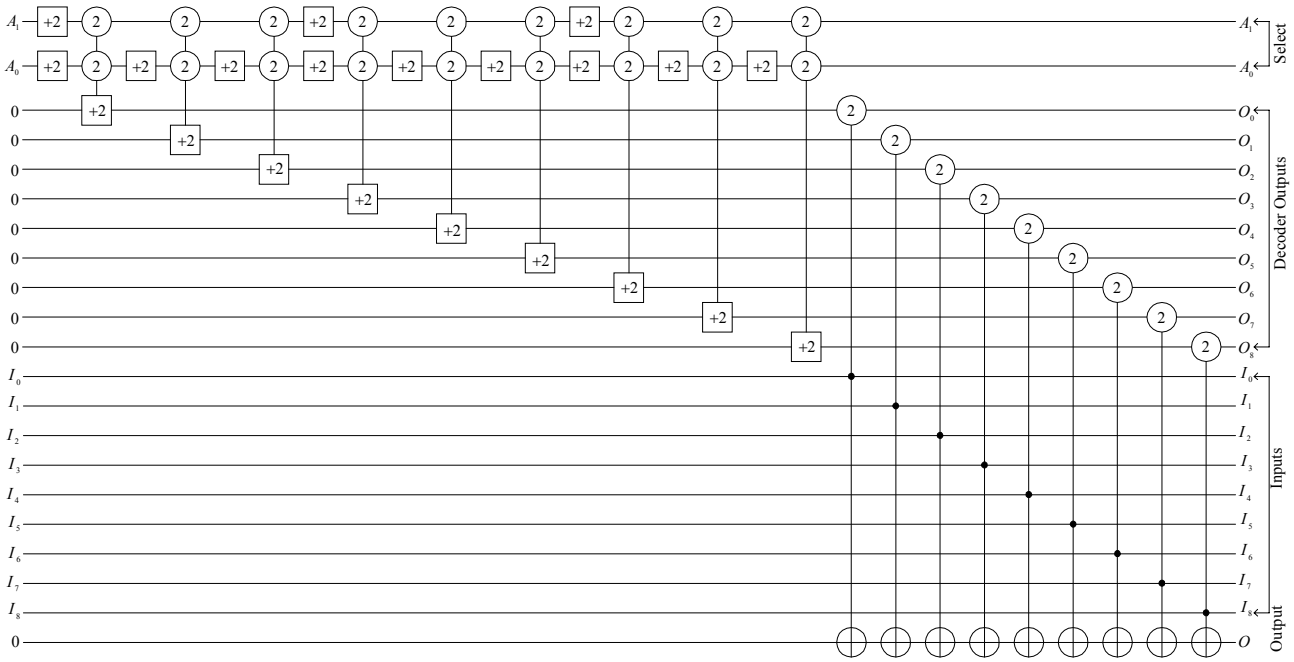

Figure 7. Realization of a 9×1 ternary reversible multiplexer [cost = 102].

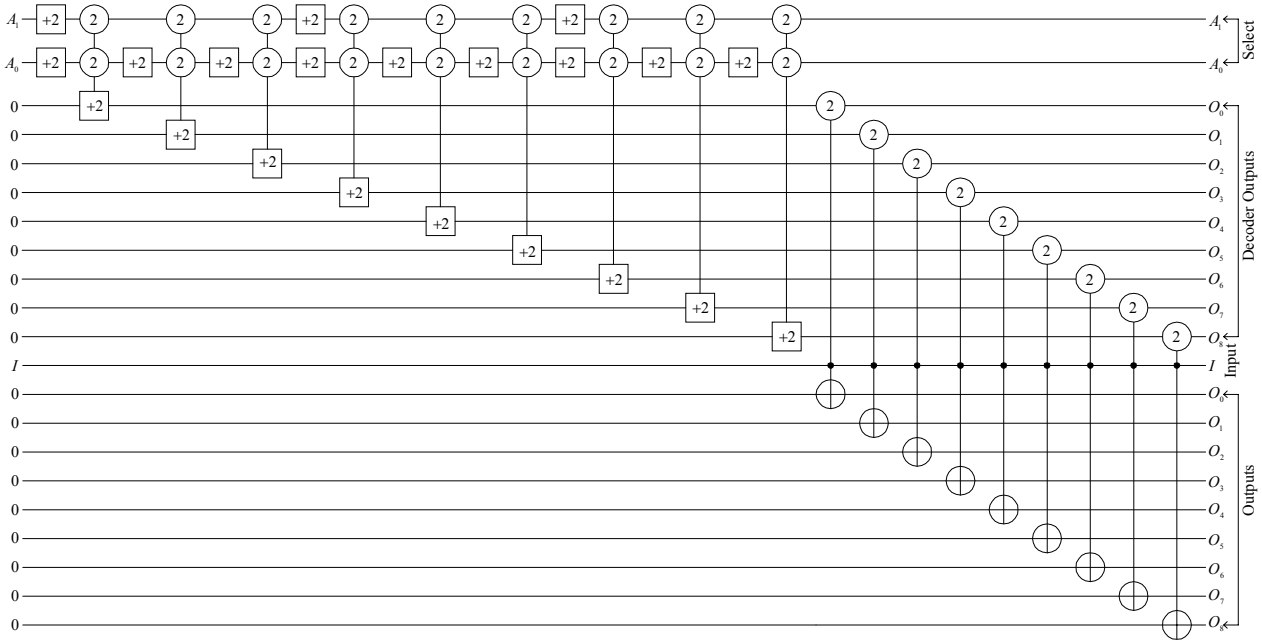

Figure 8. Realization of a 1×9 reversible demultiplexer [cost = 102].