A High Driving Capability CMOS Buffer Amplifier for TFT-LCD Source Drivers

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Abstract—A high driving capability CMOS buffer amplifier with high slew-rate, low power, and low offset voltage for high resolution TFT-LCD source drivers is proposed. Low power and high driving capability are achieved by using a telescope-cascode based complementary differential input stage combing with a common source push-pull stage and two auxiliary driving transistors. The designed buffer amplifier attained 20 V/μs and 18 V/μs rising/falling slew-rates, 1 μA static current, and 2.5 mV offset voltage for 1 nF load capacitance with a supply voltage of 3.3 V. The settling time is only 1.62 μs even the load capacitance is up to 5 nF.

***Index Terms*—TFT-LCD driver, source driver, buffer amplifier, slew-rate.**

I. Introduction

As the display resolution increases, the load capacitance of buffer amplifier increases, whereas the required settling time decreases. Beside that, large number of buffer amplifiers built into a single chip creates power dissipation problem. Consequently, a high driving capability buffer amplifier with low static power consumption is indispensable [1]. In order that the TFT-LCD displays beyond 512 gray levels each color, each gray level is required to be less than 6.4 mV for a 3.3 V full scale. Therefore, the output buffer must have an offset voltage less than ±3.2 mV [2].

There are many works on LCD drivers [1-4]. As reported in [1], [3-5], the static power consumption of a folded-cascode amplifier is larger than that of a telescope-cascode one for more current summing circuits and tail current. Also the maximum efficiency of a folded-cascode amplifier is less than 50 percent [6], and thus has poor driving capability. The offset voltages of the folded-cascode operational amplifiers described in [1], [4], are 10 mV and 12.2 mV, respectively. These reported offset voltages are too high that will create incorrect activation for gray level above 512.

As mentioned in [1], [7], a buffer with complementary differential pair is able to deliver larger current and thus have better driving capability. In order to achieve higher driving capability with low static power and low offset voltage, we design a newly developed telescope-cascode based buffer amplifier with complementary differential input stage for low power and high resolution applications. Low offset voltage and high driving capability are attained further by a designed pair of auxiliary driving transistors [3].

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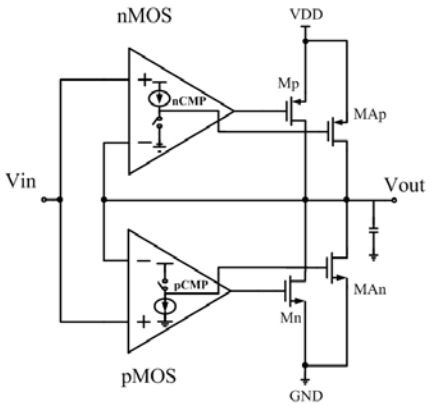
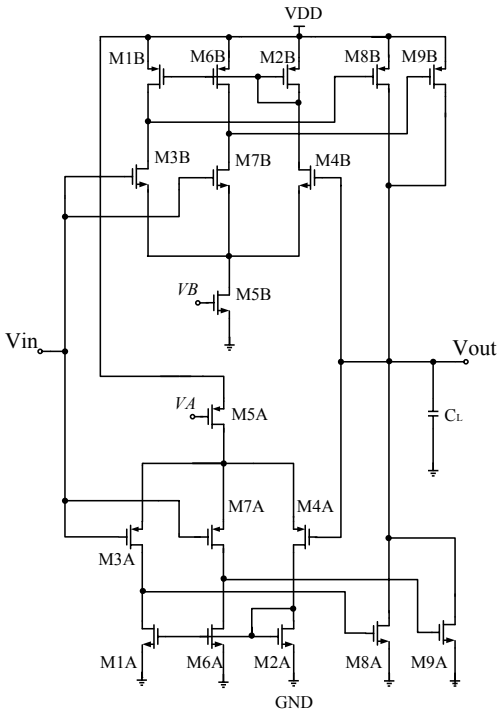
II. Proposed Circuit and Operation

The designed buffer amplifier with two complementary differential input amplifiers is shown in Fig. 1(a). The circuit was formed by a common-source push-pull stage, Mn and Mp, which offers good swing characteristics. In order to increase the driving capability, a pair of auxiliary driving transistors, MAp and MAn, are introduced and controlled by two comparators, nCMP and pCMP. The added comparators are merged with the original differential amplifiers to further reduce the power dissipation. Fig. 1(b) shows the detailed circuit of the buffer amplifier. In that, transistors M1A-M5A and M1B-M5B form the complementary telescope-cascode differential stages. The inputs of these stages are connected in parallel. Each of them drives one half of the common-source push-pull stage, M8A(B). In the figure, M5A(B) forms the biasing current source, while M6A-M7A and M6B-M7B are two sets of comparators and M9A(B) is the auxiliary driving transistor.



(a)



(b)

Fig. 1. (a) Block diagram and (b) circuit diagram of the proposed buffer amplifier.

Transistors M1A-M7A and M1B-M7B of the input differential pair are active when *Vin* reaches the center of the supply voltage. Their biasing currents are determined by *VA* and *VB*. We choose longer length for transistor M5A(B) to reduce the channel length modulation and to the systematic offset. For the input differential amplifier, the W/L of M3A(B) is chosen the same value as that of M4A(B), but the aspect ratio of M7A(B) is designed smaller than that of M3A(B), while transistors M1A(B), M2A(B), and M6A(B) are designed to have the same sizes. The currents of M3A(B) and M7A(B) can be expressed as

$$\begin{aligned} I_{M7A(B)} &= \frac{1}{2}\mu_{p(n)}Cox(\frac{W}{L})_7(V_{SG}-|V_t|)^2 \\ &= \frac{1}{2}\mu_{p(n)}Cox[(\frac{W}{L})_3-\Delta\frac{W}{L}](V_{SG}-|V_t|)^2 \\ &= I_{M3A(B)}(1-\Delta\frac{W}{L}) \end{aligned} \quad (1)$$

The current through M7A(B) is smaller than that through M3A(B), that will drive M6A(B) in the triode region and force $V_{DS6A(B)}$ close to 0 V. The auxiliary driving transistor M9A(B) will then stay off and consume no static power in that state. Hence, the aspect ratios of the auxiliary driving transistors can be designed with larger values to obtain higher driving capability without increasing power consumption. Meanwhile, higher aspect ratio of the output stage than that of the input stage can be designed to achieve lower offset voltage [8].

Fig. 2 shows the output responses of these two buffer amplifiers without and with auxiliary driving transistors, loading with a 1nF capacitor. It can be observed in the figure that the charging capability is greatly improved for the latter one. For the settling times being defined as the time required for the output signal reaching within 0.2% of the final voltage, the simulated settling times shown in Fig. 2 for the rising edges of cureves A and B, represented for the cases without and with auxiliary driving transistors, are 3.1 μs and 0.4 μs, respectively.

Defining $R_{8A(B)}$ and $R_{9A(B)}$ as the channel resistances of the output transistor M8A(B) and the auxiliary driving transistor M9A(B), respectively, the output response of the rising edge can be expressed as

$$Vout = V_I + (V_F - V_I)[1-\exp(-\frac{t}{\tau_p})] \quad (2)$$

where V_I and V_F are the initial and final values of the output voltage, respectively, and

$$\tau_p = (R_{8B} // R_{9B}) \times C_L \quad (3)$$

where C_L is the load capacitance of the buffer amplifier. The positive slew-rate can then be expressed as

$$\left.\frac{dVout}{dt}\right|_{t=t_1} = \frac{(V_F - V_I)}{\tau_p}\exp(-\frac{t_1}{\tau_p}) \quad (4)$$

From the above equations, it can be observed that the slew rate can be increased by reducing τ_p, i.e., reducing the channel resistances of the output stage, R_{8B} and R_{9B}, if load capacitance is constant. In a similar way, we can increase the negative slew-rate by reducing the channel resistances of R_{8A} and R_{9A}. Fig. 3 shows the simulated slew rates versus load capacitances (500 pF-5 nF) with 3 V output voltage. Simulated result shows a possible slew rate higher than 18 V/μs for load capacitance less than 1 nF. The simulated offset voltages versus input voltages are shown in Fig. 4, where the maximum offset voltage is 2.2 mV for the input range 0.2-3 V.

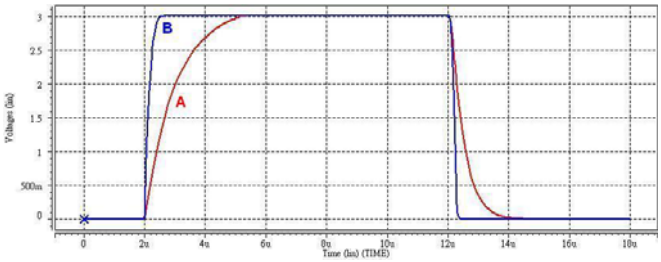


Fig. 2. Traces A and B are the output responses of the buffer amplifiers without and with auxiliary driving transistors, respectively, with 3 V voltage swing and 1nF load capacitance.

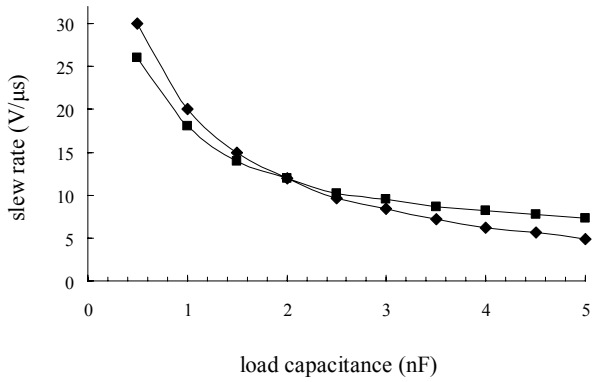


Fig. 3. Simulated slew rates versus load capacitances with 3 V output voltage.
□ rising edge ▪ falling edge

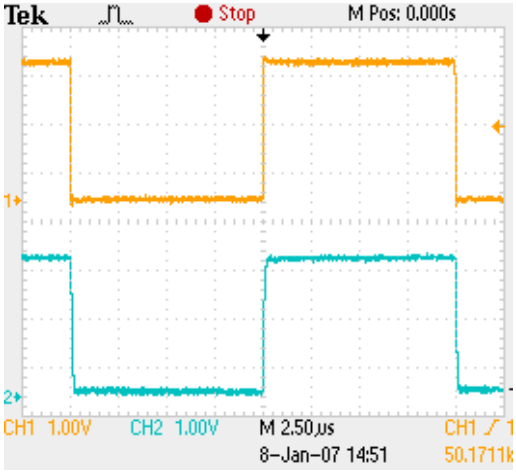


Fig. 5. The measured result of the proposed buffer amplifier under a 50 KHz step input waveform with an amplitude of 3 V and 1 nF load capacitance.

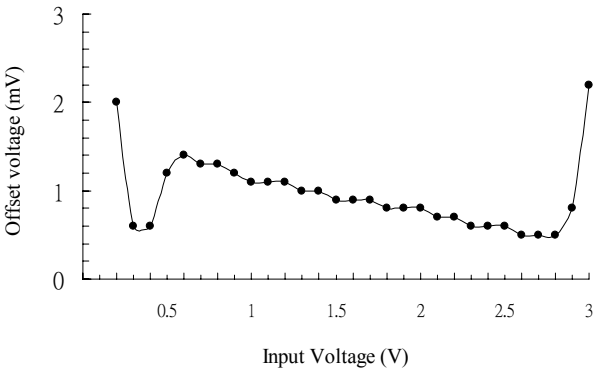


Fig. 4. Simulated offset voltages versus input voltages.

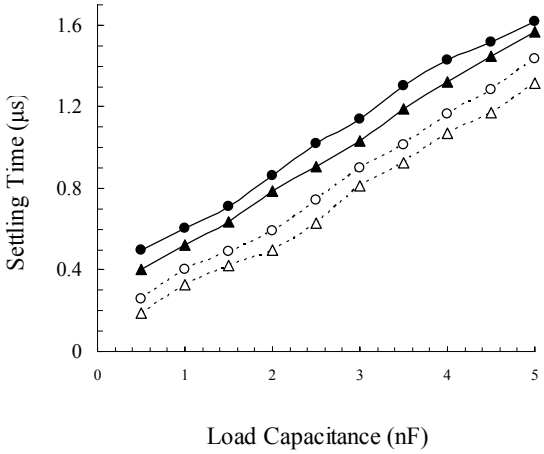


Fig. 6. The measured and simulated settling times for various load capacitances with 3 V voltage swing.
□ rising edge (simulation) ○ falling edge (simulation)
▲ rising edge (measurement) • falling edge (measurement)

III. Experimental Results

The proposed output buffer amplifier was fabricated using the TSMC 0.18μm CMOS process. Several measurements have been done. The measured static current of the output buffer is 1 μA from a 3.3 V supply voltage. The maximum offset voltage is 2.5 mV, and the slew rate is higher than 18 $V/\mu s$ for 1 nF load capacitance. Fig. 5 shows the measured result of the proposed buffer amplifier under a 50 KHz step input waveform with a 3 V amplitude and 1 nF load capacitance. Fig. 6 shows the measured and simulated settling times for various load capacitances with 3 V voltage swing. It is worth mentioned that the settling time is only 1.62 μs even the load capacitance is up to 5 nF. The die photograph is shown in Fig. 7. Since the designed circuit is rather neat, the size of the buffer amplifier is only 38 μm × 40 μm. The performance of the proposed buffer amplifier is summarized and compared with the other reported circuits in Table I. It can be observed from the table that the proposed buffer amplifier has a superior performance than that of the other circuits on slew rate, settling time, offset voltage, and static current.

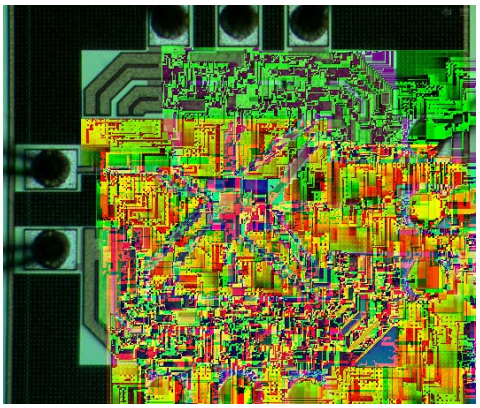


Fig. 7. Die photograph of the designed buffer amplifier.

TABLE I PERFORMANCE COMPARISONS

Parameters	This work	[1]	[3]	[4]
Process	0.18 μm	0.35 μm	0.35 μm	0.35 μm
Supply voltage (V)	3.3	3.3	3.3	3.3
Load, CL	1 nF	1 nF	680 pF	600 pF
Slew rate + (V/μs)	20	11	8	4.8
Slew rate - (V/μs)	18	7	6.5	4.7
Offset (mV)	2.5	10	N/A	12.2
Static current (μA)	1	1	4.5	7
Settling rising time(μs) falling time(μs)	 0.3 0.4	N/A	 1.2 1.4	 2.7 2.9

IV. Conclusion

In this paper, we have designed and demonstrated a high driving capability CMOS buffer amplifier with low static power, and low offset voltage, which is suitable for the source drivers of high resolution TFT-LCD with gray levels above 512. The well designed telescope-cascode based buffer amplifier consumes only 1 μA static current and achieves 18 V/μs slew rate for 1 nF load capacitance. Thus, the buffer amplifier is quite promising for high resolution flat-panel displays that require low static power, high driving capability and high accuracy.

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