# Hybrid Architecture of Genetic Algorithm and Simulated Annealing

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Abstract—This paper discusses novel dedicated hardware architecture for hybrid optimization based on Genetic algorithm (GA) and Simulated Annealing (SA). The proposed architecture achieves high speed processing. Moreover, it achieves the searching not only globally, but also locally. To keep general purpose, self-control processing by a handshake system is introduced. By adopting the handshake system, the proposed architecture can be applied to various combinatorial optimization problems by only changing an encoder, a decoder, and an evaluation circuit. Furthermore, the proposed architecture realizes flexibility for many genetic operations on GA. In order to evaluate the proposed architecture, we conduct two kinds of experiments. One is an experiment which applies the proposed architecture to TSP, and the other is an experiment which applies it to VLSI floorplanning. These experiment results prove that the proposed architecture achieves high speed processing, while keeping the quality of the solutions.

*Index Terms*—Genetic algorithm, Simulated annealing, Dedicated hardware, General-purpose properties

#### I. INTRODUCTION

Genetic Algorithm (GA)[1] was proposed by Holland as an algorithm for probabilistic search, learning, and optimization, and is based in part on the mechanism of biological evolution and Darwin's theory of evolution. This algorithm is a powerful search tool, particularly when applied for combinatorial optimization problems[2]-[7]. However, the implementation of an efficient GA often faces two major problems, on one side, the premature convergence to local optima and on the other the requirements for the GA search of long times in order to reach an optimal or a good suboptimal solution.

In order to prevent the premature convergence, the coupling of GA and one point search algorithm (local search algorithm), such as Simulated Annealing (SA)[8]-[11], to form hybrid GA can be advantageous. SA repeatedly generates succeeding solutions using the local search procedure. Some of them are accepted and some will be rejected, according to a predefined acceptance rule. The acceptance rule is motivated by an analogy with annealing processes in metallurgy as shown in Fig.1 (a).

On the other hand, GA repeatedly propagates generations

for a large population by applying three operators, which consist of selection, crossover and mutation as shown in Fig.1 (b). Therefore, GA requires the long computational time. The dedicated hardware for genetic algorithm processing is an important in order to reduce processing time.

In this paper, we propose the new dedicated hardware architecture for hybrid optimization based on GA and SA. It achieves the searching not only globally, but also locally. To keep general purpose, self-control processing by a handshake system is introduced. By adopting the handshake system, the proposed hardware can be applied to various combinatorial optimization problems by only changing an encoder, a decoder, and an evaluation circuit. Furthermore, the proposed hardware realizes flexibility for many genetic operations on GA. In order to evaluate the proposed hardware, we conduct two kinds of experiments. One is an experiment that applies the proposed hardware to TSP, and the other is an experiment that applies it to VLSI floorplanning. These experiment results prove that the proposed hardware achieves high speed processing, while keeping the quality of solutions.



Fig.1 One point search and population based search

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# II. PRELIMINARIES

## A. Traveling Salesman Problem and coding

Traveling Salesman Problem (TSP)[12],[13] is one of the most basic combinatorial optimization problems. Regarding TSP, given a set of n cities and the travel cost between each pair of cities (usually distance), the salesman is to visit each once, and finally return to the start city. Therefore, a solution is an order of visiting the cities. Fig.2 shows an example of coding in TSP.



Fig.2 Example of coding in TSP

Here, if one-point crossover and multi-point crossover are adopted in this coding, it generates many lethal genes. Fig.3 shows an example of the one-point crossover procedure and the offspring generated by the crossover. In relation to one offspring ( $C^X$ ), genes of "C" and "E" are overlapped, and conversely genes of "D" and "F" are lacked in this example. The overlap and lack indicate lethal genes. The other offspring ( $C^Y$ ) is also the lethal genes as well as  $C^X$ . In case of  $C^Y$ , genes of "D" and "F" are lacked. Therefore, several crossover operators were proposed in order to prevent generating lethal genes.



Fig.3 Example of one-point crossover

Grefenstette *et al.* [14] proposed a coding technique using a visiting city list which is created as preprocessing. An individual is represented by an order of a list instead of city name. Fig.4 shows an example of an encode procedure of Grefenstette's approach, before crossover operation. And then, Fig.5 shows an example of one-point crossover using the encoded chromosomes. Thus, it can prevent generating lethal genes if one-point crossover and multi-point crossover are adopted. A decode procedure also requires after crossover operation. Fig.6 shows an example of the decode procedure.





$\mathbf{P}^{\mathbf{X}}$	3 4 4 6	13	2	1	
$P^{\scriptscriptstyle Y}$	4 6	1 1	1	1	
		¥			
$C^{x}$	3 4	1 1	1	1	
$\mathbf{C}^{\mathrm{Y}}$	4 6	1 3	2	1	

Fig.5 Example of one-point crossover using encoded chromosomes



Fig.6 Example of decode procedure

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# B. VLSI floorplanning problem

Floorplanning[3],[15] is a generalization of the placement problem in VLSI building block layout, and it determines the coarse placement for the given set of modules. The objective of floorplanning is that (1) no modules overlap, (2) the packing area and interconnection costs are minimized. The sequence pair [15] was proposed as a representation method of floorplanning, achieving a measure success.

A sequence pair is an ordered pair of  $\Gamma$ + and  $\Gamma$ -, where each of  $\Gamma$ + and  $\Gamma$ - is a permutation of the names of given *n* blocks. Fig.7 shows a floorplan and a relative position of each block of one. Given ( $\Gamma$ +,  $\Gamma$ -), one the optimal packing under the constraint can be obtained by applying the well known "longest path algorithm" for vertex weighted directed acyclic graphs (horizontal and vertical constraint graph) as shown in Fig.8.

#### C. Previous work

Examples of dedicated GA hardware to reduce processing time have been reported by Scott *et al.*[16], Graham *et al.*[17], and Imai *et al.*[18]. Scott *et al.* developed a hardware-based GA and demonstrated its superiority to software in speed and solution quality. Imai *et al.* proposed a processor element constituting parallel GA, and achieved the parallelism due to the number effect.

However, most of these previous works deal with small-scaled problems and limit to some fixed genetic operations. Thus, no studies have been performed to develop a dedicated hardware to realize hybrid searches that combine GA with SA.

# III. ARCHITECTURE METHODOLOGY

The proposed hardware has several merits: (1) hybrid optimization of GA and SA, (2) realization of high general-purpose properties, (3) introduction of a hardware-oriented hybrid algorithm, and (4) adoption of an architecture combining GA and SA.



Regarding (1), GA is inadequate in relation to a systematic search near a good solution, because it generates a new search point focusing on crossover calculation. Conversely, one point search algorithm, such as SA, is excellent in a local search processing, however, its global search is inadequate. Hybrid search combines algorithms having such complementary relationships, so the ability to search for a solution is improved.

Several proposals on hybridization have been made [19]-[28] in which the one-point search is made for a systematic search near a good solution and the GA conducts the global search. Therefore, the proposed hardware realizes hybrid optimization using GA and SA. Fig.9 shows the processing flow of the proposed one.



Fig.9 Processing flow of the proposed hardware

Regarding (2), in the proposed hardware, self-control processing by a handshake system is introduced. In this self-control processing, each circuit has a request signal and an acknowledge signal as an enable signal. By introducing this type of handshake system, the timing design of each circuit becomes independent, and consequently, high general-purpose properties can be realized. Thus, the proposed hardware can be applied to various combinatorial optimization problems by only changing an encoder, a decoder, and an evaluation circuit as shown in Fig.10. Regarding genetic operations, roulette wheel selection, ranking selection, and tournament selection are realized as the selection operator, and swap operation and inversion operation are realized as the mutation operator, in order to realize general-purpose properties similar to software processing. That is, the evolution strategy most suitable for various problems can be selected.

Regarding (3), a new SA algorithm is introduced, in which calculation cost is reduced maintaining the accuracy of the solution. The proposed algorithm adopts a new hardware-oriented calculation technique instead of the calculation of exponential function which is used in conventional SA.



Fig.10 High general-purpose properties

Thus, the proposed hardware achieves not only high speed processing, but also reduction of calculation steps.

Regarding (4), the proposed hardware adopts a combined architecture that shares a circuit to perform local search processing of SA and a circuit to perform mutation processing of GA. By adopting this new combined architecture, the circuit scale can be reduced.

#### IV. HARDWARE OF GENETIC ALGORITHM

For GA, it is important to set suitable evaluation parameters for controlling the selection of individuals. The selection operations are implemented as roulette wheel selection and ranking selection.

The roulette wheel selection method uses the percentage represented by the evaluation value for each individual with respect to the sum total of evaluation values for all individuals are the selection probability for each individual. As a result, if the evaluation value for the *i*-th individual is f(i), then a roulette wheel showing this percentage as a wedge can be used, as shown in Fig.11.

To put this concretely, let us consider the case of the evaluation values shown in Fig.12 (a). First, the product of the individual evaluation values is calculated in alphabetical order, as shown in Fig.12(b). Next, a random number taking a value in the range of "0" to "product of the evaluation values for all individuals" is generated. For Fig.12 (b), if the generated random number is from "0" to "99", individual A will selected. And then, if it is from "100" to "399", individual B will be selected. The Roulette wheel selection runs in this fashion.

In relation to the Ranking selection, this method attempts to preserve descendants using a probability determined for each initial rank assigned to individuals by using the evaluation value. To put this in concrete terms, let us consider a case in which there are four individuals with the evaluation values shown in Fig.12 (a), and with the selection probabilities shown in Fig.12 (c). First, the product of the selection probability is calculated in descending rank as shown in Fig.12 (d) as a form of preprocessing (performed only once for the first generation). Next, individuals are sorted in descending order for the evaluation value. As is illustrated in Fig.12 (e), the sorted individuals correspond to the products of the selection probability in Fig.12 (d). Then random numbers are generated in the same fashion as seen in the Roulette wheel selection, and the ranking selection is implemented by selecting individuals.

### V. HARDWARE OF SIMULATED ANNEALING

In a conventional SA, the calculation of exponential function is required for the acceptance criterion. However, this calculation requires not only a very large number of calculation steps, but also a lot of hardware resources. To reduce the calculation steps and hardware resources, a new hardware-oriented SA algorithm is introduced in the proposed hardware.

The algorithm for the acceptance criterion of the proposed hardware-oriented SA algorithm is as follows.



Fig.11 Example of roulette wheel

individual	Α	В	С	D
Evaluation Value	100	300	150	50

(a) Evaluation values for individuals

Prod	uct 1	00 -	400	550 <u>60</u> 0
	Α	В	C	D

(b) Product of evaluation values

Ranking	1	2	3	4
Selection probability	40%	30%	20%	10%

(c) Selection probabilities for individuals



(d) Product of selection probabilities



(e) Correspondence between selection probability and individual

Fig.12 Processing flow of the proposed hardware

$$\begin{cases} P = \frac{1}{X+1} \\ X = \frac{\Delta E}{T} \end{cases}$$
(1)

Where, P represents the ratio of acceptance of the deteriorated solution, delta E represents the difference of energy, and T represents temperature.

As a result, the calculation steps and the hardware resources can be reduced by adopting the proposed SA algorithm.

# VI. CIRCUITS

The block diagram of the proposed hardware is shown in Fig.13. It consists of selection circuit, mutation circuit, crossover circuit, memory controller, generation management circuit, serial communication circuit, evaluation circuit, FPGA (Filed Programmable Gate Array) board interface circuit, and SRAM. Moreover, the proposed hardware introduces the self-control circuit in each sub circuit as shown in Fig.13. The self-control circuit is required for the handshake of data communication in each circuit and improves independence of each sub circuit.



Fig.13 Block diagram of the proposed hardware

#### VII. EXPERIMENT AND DISCUSSION

To evaluate the proposed hardware, we applied it to TSP problem and VLSI floorplanning problem. The proposed hardware has been designed by Verilog-HDL and synthesized by the Synplicity Synplify. The clock frequency of the proposed hardware is set up with 20 MHz. Table.1 shows the gate size. EBS indicates memory blocks of FPGA in Table.1.

We simulate the performance of the proposed hardware with the number of steps and compare it with software processing. The experimental data of TSP problem is TSP.LIB benchmark data (eil51:51 cities), and that of VLSI floorplanning is original data(50 blocks).

The software processing was implemented in the C language and run on a Linux PC. The clock frequency of the Linux PC is 2.4GHz. In these experiments, both the software processing and the hardware processing run until the 2000th loops in SA and the 20000th generation in GA.

Table.2 shows the comparison results. In TSP problem, the proposed hardware improved the speed of 22% in comparison with software processing. Moreover, in VLSI floorplanning problem, it achieved seven times speed-up compared with software processing. The clock frequency is 20MHz for a limit of FPGA in this research. However, the proposed hardware is speeded up more, if it is implemented on LSI (Large Scale Integration).

TABLE.1	GATE	SIZE

Circuit name	Logic resource (%)	EBS (%)
Generating management	1	1
Memory controller	8	15
Selection	50	28
Crossover	7	5
Mutation	8	2
Evaluation (TSP)	24	92
Evaluation (floorpalnning)	59	8

TABLE.2 COMPARISON RESULTS				
Software(s) Hardware(s) Times				
TSP	10.54	8.69	1.21	
Floorplanning	223.32	28.77	7.76	

## VIII. CONCLUSION

In this paper, we proposed the new hardware architecture for hybrid optimization based on Genetic Algorithm and Simulated Annealing. The hybrid optimization of GA and SA in the proposed hardware achieved searching not only globally but also locally. To keep general purpose, the proposed hardware realized flexibility for many genetic operations on GA. Moreover, the gate size of the proposed hardware was reduced by adopting the combine architecture of GA and as SA. Simulation results proved that the proposed hardware achieved high speed processing as compared with software processing. In relation to future works, we will expand the architecture to the artificial intelligence chip.

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