# Preface to the Special Issue on
# High Performance Reconfigurable Systems

**Special Issue Guest Editor:**
Dr. Khaled Benkrid - Lecturer at the University of Edinburgh, Scotland, UK

It gives me a great pleasure to introduce this IAENG Engineering Letters' special issue on high performance reconfigurable systems, which aims to present the latest developments in the field of high performance reconfigurable computing, be it on the architectural level, the application level, or the design/programming tool level.

The first paper in this special issue presents a recent novel development in the realm of high performance reconfigurable computing systems, in the form of the Maxwell FPGA supercomputer built by the FPGA High-Performance Computing Alliance at the University of Edinburgh in Scotland, UK. Maxwell is a general-purpose 64-node FPGA computer designed for high-performance parallel computing. The paper describes the machine architecture, its hardware and software eco-system, as well as a number of initial benchmarks.

Following on this, the following two papers present two relatively recent application domain implementations on FPGAs, namely financial computing, and bioinformatics and computational biology. The first paper presents a high performance FPGA implementation of a generic Monte-Carlo simulation engine for financial computing, with an actual hardware implementation on the Maxwell machine resulting in up to three orders of magnitude speed-up compared to an equivalent software implementation. The second paper presents the first ever reported FPGA implementation of an important biological sequence alignment algorithm, namely the Gapped BLAST sequence alignment with the two-hit method. This implementation results in, at least, one order of magnitude speed-up compared to software, on a single FPGA chip.

The following paper in this special issue deals with an important application of reconfigurable hardware, namely the construction of fault-tolerant systems. The paper presents a cross-cubed topology for parallel computing systems which allows for higher robustness against faulty nodes. The dynamic adaptiveness of such networks is particularly important to modern VLSI systems as transistor integration levels continue to decrease to atomic levels.

The final paper in this special issue looks at the design/development tools' side of reconfigurable systems as it presents a logic based hardware development environment particularly suitable for Intellectual Property (IP) core development in reconfigurable System-on-Chip (SoC).

I do hope that you will find this special issue enjoyable, informative and useful to your research.

**Dr. Khaled Benkrid** holds an Ingenieur d'Etat in Electronics Engineering from Ecole Nationale Polytechnique d'Alger, a PhD in Computer Science, and an Executive MBA from Queen's University Belfast, UK.

He is now a Lecturer in the School of Engineering and Electronics at the University of Edinburgh, Scotland, UK, after having spent six years as a Lecturer in Computer Science at Queen's University Belfast. With over ten years experience in reconfigurable hardware design, he has authored over 50 publications in major international journals and conference papers in the areas of high performance reconfigurable computing and electronic design automation. He continues to be active in these areas with applications in digital signal processing, bioinformatics and computational biology, and scientific computing.

Dr. Khaled Benkrid is a Senior Member of IEEE and a Chartered UK Engineer. He has served as program committee member and session chair at many international conferences including the IEEE 2004 ISVLSI conference, the 2007 NASA/JPL AHS conference, and the 2008 WorldComp ERSA conference. He is the holder of various research grants from the UK government, the EU, and Industry.