A Review on Design Considerations & Limitations of Resonant Gate Drive Circuit in VHF Operations

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***Abstract*—A comprehensive review of resonant gate drive (RGD) circuits operating in very high frequency (VHF) switching is discussed. The specific RGD circuits are normally applied only for certain applications due to their design limitations and drawbacks. The isolation techniques must be considered to avoid mismatch and interruption of signals as well as the dead time delay, size of components and choice of optimized parameter values. Low conduction losses and higher switching speed are important in achieving high efficiency of the driver. A new RGD circuit is proposed using power MOSFET device to show its robustness in achieving low conduction loss and high switching speed. In the near future, high power GaN HEMT can be used as a substitute for power MOSFET switch in VHF switching operation. Even though this device is not yet commercially available, the simulation study on RGD circuits can be realized through modeling. Studies have shown that some RGD circuit designs using power MOSFET can be modified and replaced with this device. However, the investigation on circuit performance and reliability on signal integrity have to be further investigated due to their differences in semiconductor properties and electrical characteristics.**

***Index Terms*—**GaN HEMT, Isolation Technique, Power MOSFET, RGD Circuit, VHF Switching

I. Introduction

Gate drive circuit is important in the activation of on and off signals to the switch. Without careful attention in the design, improper generation of switching pulses will occur. At very high switching frequency (VHF), the effect of gate drive on overall performance and efficiency of converter becomes critical. Further increase in frequency can degrade power density [1]. Most of high frequency applications use the silicon based devices such as Insulated Gate Bipolar Transistor (IGBT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET). In discrete and Surface Mount Device (SMD) implementation, MOSFET is now chosen to be the best switching device as it can switch effectively at high frequency. However most of them only operate at most of 1 MHz for high voltage applications. Beyond that, new types of switches are required to serve the purpose. Examples are Gallium Arsenide (GaAs), Silicon Carbide (SiC) and Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) devices of which are from the III-V semiconductor group.

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II. Gate Drive Circuit Technology

In general, designing gate drive circuits requires precise consideration in getting the signal and power to the gate of the power MOSFET so that this input energy is sufficient for conduction. Most of the time, this gate drive circuit design has limiting factors between the level of voltage applied to the gate and the level of switching frequency required for the switch. The limitations include determination of the propagation or dead time delay in the switching transition, T_d, the size of the transistor and isolation techniques used to control the signal between the input source and the power MOSFET.

A. Basic Gate Drive Circuit Topologies

There are 3 types of basic gate drive topologies. They are: voltage driven, current driven and resonant topology as shown in Fig. 1(a), (b) and (c) respectively [2]. First, in voltage driven topology, large energy will be dissipated and since there is no energy recovery, thus, this topology is not suitable for high frequency operation. Power dissipation, P_v is given by:

$$Pv = fsCgVs^2 \quad (1)$$

where C_g is the gate capacitance of power MOSFET and V_s is the input voltage source. From Fig. 1(a), the maximum value of R_v which is equals to $\Delta t / 1.6\, fsCg$ is determined by required switching speed whereas the minimum value, by internal gate capacitance, C_g. Hence, there exists a maximum operating frequency which limits the charging capability of the gate [3]. Thus, the voltage driven gate drive circuit has limited capability in operating at high switching frequency.

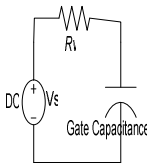

Fig. 1(a): Voltage driven

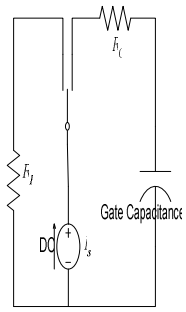

Fig. 1(b): Current driven

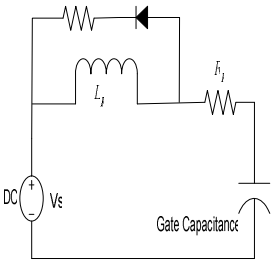

Fig. 1(c): Resonant

Secondly, in current driven topology which was initially developed by [4], the losses can be reduced significantly using voltage driven at higher frequencies. Here, less energy will be dissipated in series resistance, R_v (summation of R_c and R_F), due to freewheeling advantage of series current I_s as indicated in Fig. 1(b). Having a small inductor connected as part of current DC source, this allows for partial recovery of gate energy and reduces circulating energy loss. The $Is = \left(\frac{Vs}{2Rv} \right)$ must instead be carefully controlled using passive clamping [5] or active clamping in order to fully turn on the gate voltage and thus overcome high output impedance that makes high dv/dt. Furthermore, I_s must be one-half from of that peak voltage driven topology to ensure reduction in energy dissipation.

Thirdly, the resonant gate drive (RGD) circuit shown in Fig.1(c) implies that all energy from resonant inductor, L_R will be transferred to gate capacitance. As series resistance increases, only half of energy will be dissipated when the gate voltage reaches supply voltage. This indicates a 50% improvement. At this time, the resonant drive circuit operates in full resonance mode and this is comparable to voltage driven topology. Even though a careful measure is taken to determine which topology is suitable for the applications, obviously, there are tradeoffs between component counts, input supply type, power losses and switching frequency.

B. Gate Drive Isolation Techniques

For high voltage applications up to 1 kV, isolated power transition is required. There are several techniques which can be used for the purpose. For example, as proposed by [6, 7], the combined signal and power isolation technique is shown in Fig. 2. This technique can be a compact design; however it is not easy due to limited switching frequency capabilities of power MOSFET and the modulation design requirement. On the other hand, pulse transformer can also be used as isolation [8, 9]. Currently piezoelectric transformers are commonly utilized to establish isolated power transition but with the cost of high power dissipation.

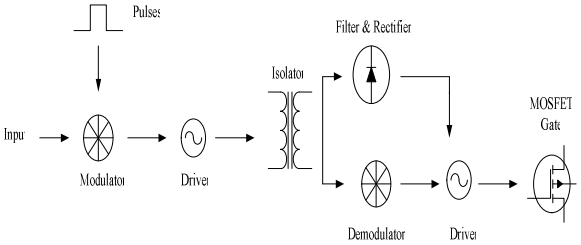

Fig. 2: Combined signal and power isolation

Another technique which is popular for higher power converters is the separate signal and power isolation technique [10, 11] as shown in Fig. 3. The technique prevents from problematic ground loops and can be made by multiple connections between gate drive circuit and power unit. It also serves as isolation between input signal and power MOSFET switch. The only problem is that the design is bulky.

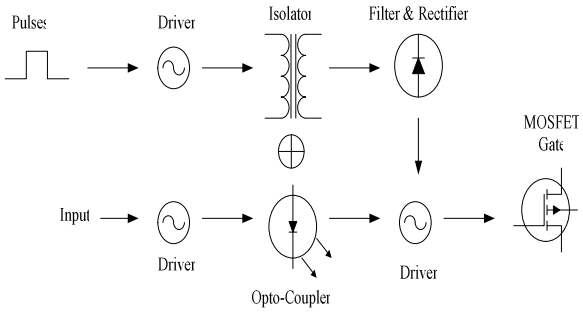

Fig. 3: Separate signal and power isolation

Signal level shifting and power bootstrap [12, 13] technique is the simplest and widely used in industry. As shown in Fig. 4, it is more suitable for low power products. However, this type of isolation technique has some drawbacks. The level shifter has the disadvantage in providing the signal as it can generate error especially due to the reverse recovery currents generated by bootstrap diode. Another problem is the difficulty in implementing the protection schemes to this technique. As a result, detailed analysis considering level shifter design must be taken seriously to avoid cross conduction of gate voltage and thus, reduce gate drive loss.

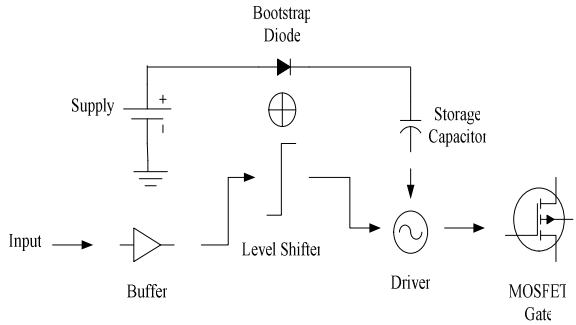

Fig. 4: Signal level shifting and power bootstrap

This eventually leads to the latest implementation of isolation technique where optical isolation is preferred. It is more compact compared to conventional galvanic method. However, optical isolation method indicates signal distortion and propagation delay when switching frequency increases in megahertz range [14, 15]. Capacitive coupling technique for cascaded switches is another technique but it not common in high voltage applications [16].

III. GATE DRIVE CIRCUIT USING VHF SEMICONDUCTOR SWITCHES

The implementation of gate drive circuit requires switching devices which can switch at its maximum frequency capability. Discrete power MOSFET device is said to be the best switching device where it can operate as far as 5 MHz for high power applications. However, it requires complex signal conditioning circuits and tradeoffs considerations. GaN HEMT is the latest switching device developed for VHF applications. It can be used in either monolithic or CMOS circuit topologies. The GHz range operation is normally for low voltage applications, but GaN can also be applied effectively in high voltage with lower frequency range ie below 5 MHz where it can be implemented on the PCB layout via either discrete or hybrid discrete-surface mounts. Both implementations still require further improvement in gate drive losses, especially in high voltage and current applications. This indicates that by increasing the gate drive loss may offset advantages gained by lower conduction losses of the switches [17].

A. Power MOSFET Gate Drive Circuit

The RGD circuit is designed only for specific applications and sometimes may not for others. For example, a certain design approach must be taken for the Synchronous buck converter (SBC) circuit but not for other applications. Since the circuit has two switching devices, the applicable RGD circuits are designed to tailor the need for that circuit. Coupled inductors can be used to drive both switches using one magnetic core [18]. This minimizes the size of RGD circuit and helps transfer the energy between switches to improve performance and efficiency.

Until now, many studies have been conducted for RGD circuits' improvement and yet are still in further development. Most of the studies utilize a LC resonance technique to charge power MOSFET gate capacitance. This gate capacitance charges and discharges during the switching stage and thus significant energy losses are dissipated. Consequently, some of the energy from these losses of which mainly come from the gate capacitance must be recovered. In addition, the RGD circuit that has the inability of fast cycle dynamics will not be suitable for high frequency applications with rapid loads transients. Here, the isolated pulse RGD circuit reported in [19], had the difficulties in controlling the power MOSFET gate voltage, V_{gs}. It depends on the gate capacitance and pre-stored energy in inductor which leads to floating gate voltage and false triggering of switches. This RGD also suffers from voltage oscillation after it turns off. At present, most driving techniques use discrete inductor or transformer windings [20-23], while others use leakage inductance [24]. Leakage inductance results in faster driving speed but usually varies based on manufacture variations. In general, the requirement of good RGD circuit for VHF applications can be summarized as follows:

a) Ability to have fast duty cycle dynamics.
b) Gate impedance of the switching device should be low after turning on and off to prevent false triggering.
c) Gate voltage V_{gs} must be well controlled after turning on and off.
d) Ability to have fast gate drive speed and at the same time produce low driving power losses.

In addition, there are also several critical considerations in designing RGD circuit which are listed below.

a) Propagation delay of input signal through switches' gate terminals.
b) Pulse width distortion of input gate signal.
c) PCB layout parasitic of power converter.
d) Device switching voltage swings and related Electromagnetic Interference Immunity (EMI)
e) Determination of minimum pulse width for power MOSFET.
f) Protection features such as trip out and trip trigger input.
g) V_{ds} over-drive control to optimize efficiency.
h) Selection of gate inductance value.
i) Miller's effect and start up consideration.

Fig. 5 below shows the conventional hard switching power MOSFET gate drive circuit. The gate driving losses include capacitive power losses, P_{cap}, where it relates to power MOSFET gate charge. The others are P_{sw}, switching losses and P_{dr}, driving losses. The internal parasitic capacitance, C_{iss} is the summation of gate-drain capacitance C_{gd}, and gate-source capacitance, C_{gs}. These parasitic parameters contribute to the power losses in the gate drive circuit.

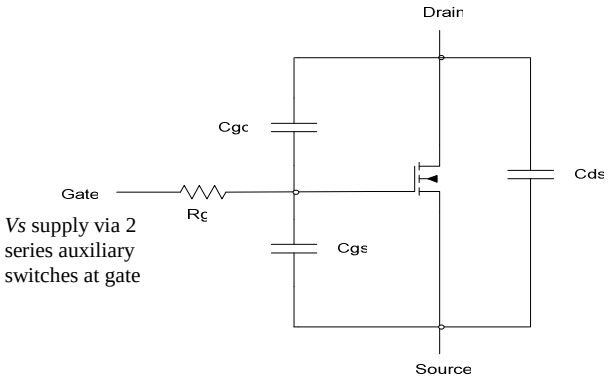

Fig. 5: Conventional Hard Switching Gate Drive Circuit

The total gate losses can be given by:

$$P_{cap} = Q_g V_g f_s \tag{2}$$

$$P_{sw} = 2C_{oss} f_s V_s^2 \tag{3}$$

$$P_{dr} = 2Q_g V_s f_s = 2V_s^2 f_s C_{iss} \tag{4}$$

where, Q_g is total charge of power MOSFET when gate is charged to V_s voltage level. C_{oss} is the equivalent output capacitance of power MOSFET that is (C_{ds} + C_{gd}). The energy required to turn on and off the power MOSFET is dissipated mostly in the resistor, R_g. This leads to the high power

dissipation in the conventional gate drive circuit. The Root Mean Square (RMS) power loss (the sum of on-conduction losses of gate drive switches, losses occurring in LC and internal gate resistance of power MOSFET) is given by:

$$P_{RMS} = V_s{}^2 C_{iss} f_s \tag{5}$$

Gate resistance, R_g limits the maximum gate current and allows this distribution of RMS losses between R_g and internal drain-source on-resistance of power MOSFET, $R_{ds(on)}$. From (3) to (5) above, power losses in auxiliary switches can be reduced by reducing C_{iss} and C_{oss}. However, increasing effective gate resistance will reduce the switching speed. The best solution is to utilize RGD circuit. Thus, there are several methods proposed to solve the power dissipation and switching speed issues.

B. Online Controllable Rise and Fall Time RGD Circuit

One of the methods is to have an online controllable rise and fall time in the RGD circuit. The circuit is shown in Fig. 6. In this method, the inductor current, I_r is first initialized prior to turning on and off which is used to charge and discharge the gate capacitance C_{iss} of power MOSFET. There are four switches involved where the resonant transition takes place during the switching cycle.

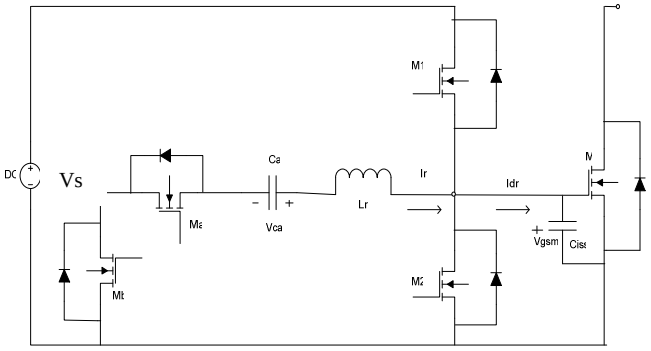

Fig. 6: Online RGD Circuit

The circuit operation and waveforms are described in details in [25]. The significant result using this RGD circuit is that some energy is recovered during both charging and discharging transitions. During turn on, the energy stored in C_a will supply to C_{iss} of power MOSFET and then return to power source. During turn off, power source energy will supply to L_r along with energy in C_{iss}. The circuit in Fig. 6 has no dependence in duty cycle of switch and it can be changed freely and has no effect on driving efficiency.

There are two types of equivalent circuits of resonant transition: one is during turn on and the other, during turn off. The circuits are shown in Fig. 7(a) and 7(b), respectively. R_{eq} is the sum of all resistance in the path. V_s is the voltage source. The initial inductor current and gate capacitor voltage are denoted as I_{L0} and V_{gs0} respectively. In Fig. 7(a), i_L (turn on stage) can be expressed as:

$$i_r(t) = (I_{r0} - \frac{V_s}{\mathrm{Re}\,q})e^{-\frac{\mathrm{Re}\,q}{L_r}t} + \frac{V_s}{\mathrm{Re}\,q} \tag{6}$$

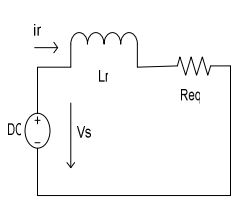

Fig. 7(a)

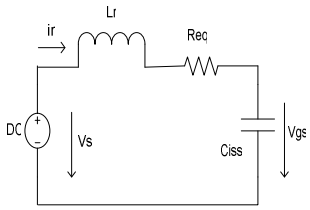

Fig. 7(b)

By solving turn off system in Fig. 7(b), i_L and V_{gs} can be expressed as:

$$ir(t) = \frac{Vs - V_{gs0} - 0.5\mathrm{Re}\,qIr0}{\omega Lr} e^{-\alpha t}\sin(\omega t) + I_{r0}e^{-\alpha t}\cos(\omega t) \tag{7}$$

$$V_{gs}(t) = \frac{1}{C_{iss}}\int_0^t i_r(t)dt + V_{gs0} \tag{8}$$

where,

$$\alpha = \frac{\mathrm{Re}\,q}{2L_r} \tag{9}$$

$$\omega = \frac{\sqrt{4L_rC_{iss} - \mathrm{Re}\,q^2}}{2L_rC_{iss}} \quad . \tag{10}$$

Then the resistive power $P_r(t)$ and diode power loss $P_d(t)$ can be given, respectively as:

$$P_r(t) = \frac{\mathrm{Re}\,q}{T_s}\int_0^{T_s} i_r{}^2(t)dt \tag{11}$$

$$P_d(t) = \frac{V_d}{T_s}\int_0^{T_s} |i_r(t)|dt \tag{12}$$

However, this RGD circuit experiences an additional stress due to the additional switches used as auxiliary. Due to the increase value of the equivalent R_{eq}, this causes a higher resistive power loss. More complex circuit is exposed in the design and hence further increase in the board size.

C. Series LCext Connection RGD Circuit

In designing a good RGD circuit, the switching frequency and duty cycle have become the primary parameters which require optimization. The switching speed of power device has to be as high as possible in order to reduce switching loss in power stage. However, the increase in switching speed will increase the power losses in RGD system. As a result, there must be an optimized switching speed (with careful design) that minimizes overall power losses especially in ZVS resonant network. Fig. 8(a) shows another type of RGD circuit which uses the role of continuous inductor current in complete cycle to charge and discharge the gate of power MOSFET [26]. The resonant inductor, L is connected in series with an external capacitor, C. Here, the capacitor is used as a DC component of voltage across L. With the requirement of this large capacitance value, this leads to the disadvantage on overall space limitation on board. The RGD circuit can operate independently with varying duty cycle and frequency. Here, a constant circulating current during switching transitions results in higher power dissipation. Despite of this drawback, the implementation of the RGD is

easy. For the design to operate, the optimization techniques have to be considered and correctly set up.

The applicable switching waveform for Fig. 8(a) is shown in Fig. 8(b). The circuit operations in details are described in details in [26]. For optimization purposes, there are two steps suggested: optimization of inductance, *L*, and calculation of an optimized $R_{ds(on)}$.

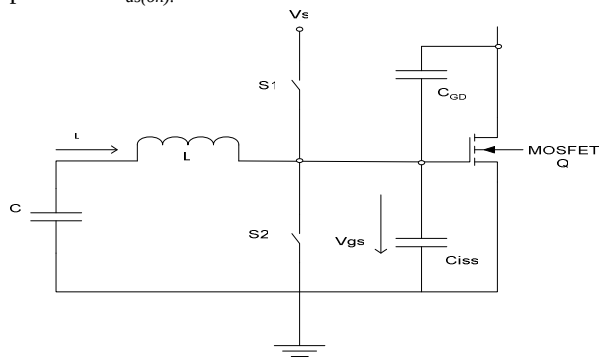

Fig. 8(a): Series LC_{ext} RGD Circuit

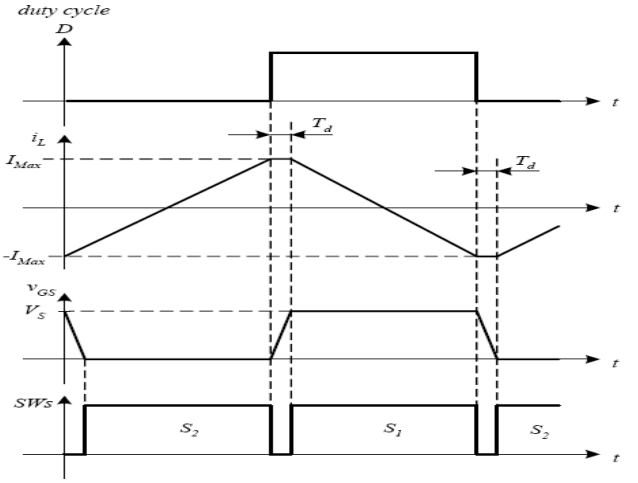

Fig. 8(b): Series LC_{ext} RGD Switching Waveforms

The first step in calculating an optimum inductance value, *L* is by knowing other input parameters. From here, the maximum resonant inductor current, I_{max} can be calculated and hence, *L*. The maximum inductor value, L_{max} must be calculated to ensure ZVS operation. However, lowering *L* will increase I_{max}, thus an increase in RMS losses while increasing *L* will eventually lower I_{max} value. As a result, this increases hard switching losses. The related formulas are expressed as

$$I_{max} = \frac{C_{iss} V_s}{T_d} \tag{13}$$

$$\left| I_{\max} \right| = \frac{(1-D)D}{2L} V_s T_s \tag{14}$$

where, T_d is the propagation or dead time delay and T_s is the a complete switching period. Once the optimized *L* is determined, then the second step proceeds. This is to calculate optimum $R_{ds(on)}$ of gate switch. Assuming that $R_{ds(on)}$ and C_{iss} product is constant in value, low $R_{ds(on)}$ value means high gate drive losses in switches. High value of $R_{ds(on)}$ results in high RMS losses. Here the optimized value of $R_{ds(on)}$ has to be carefully chosen to limit the losses. Both of these parameters can be calculated via iterative procedures or by data tabulation from mathematical model via graphical waveforms. Having known these two parameters, RGD circuit can be optimized to generate highest possible speed and lowest power losses.

IV. GaN HFET RGD Circuit

GaN comes from wideband gap material in III-V group. GaN Heterostructure Field Effect Transistor (HFET) device is suitable for VHF application especially in power amplifier circuit design. Here, the components used are mostly from monolithic and CMOS types. It is also known to have the capability in high power and temperature applications. Its switching ability allows in submicron and nanosecond range.

In the other latest development, another III-V semiconductor type, GaN HEMT device was only made in fabrication level. Currently, RGD circuits for high power GaN HEMT switches are not yet commercially available. Some RGD circuits for silicon based high switching power MOSFET can be used and modified to drive GaN HEMT switch. At the point of writing, the commercially available type of GaN device is HFET. The modified power MOSFET RGD circuit can only drive HFET only less than 5 Mhz [27]. There are challenges in the design of RGD circuit for GaN HFET. Among them are:

a) very high switching speed makes it difficult to maintain high efficiency,
b) switching power loss increases rapidly at VHF and hence reduces overall efficiency, and
c) HFET switch is ZVS-ON switching. So it needs zero voltage to turn on and a negative voltage to turn off. This control characteristic is different from P and N power MOSFETs.

The GaN HFET RGD circuit is shown in Fig. 9(a) and its switching waveforms, in Fig. 9(b) [27]. The operations are divided into several timing transitions. Referring to the waveform in Fig. 9(b), it is assumed that when $V_{gs}=V_p$-, the system begins at negative value and both auxiliary switches are off.

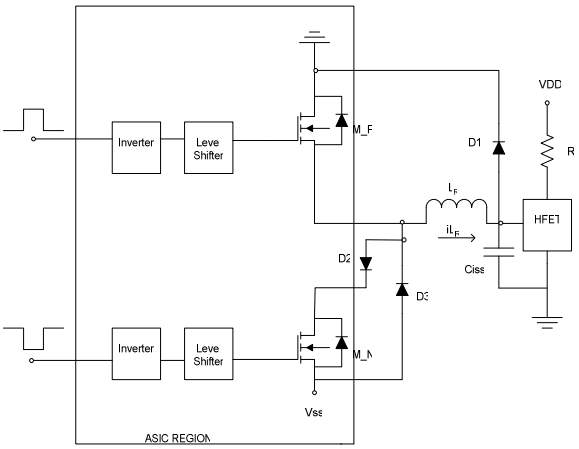

Fig. 9(a): GaN HFET RGD Circuit

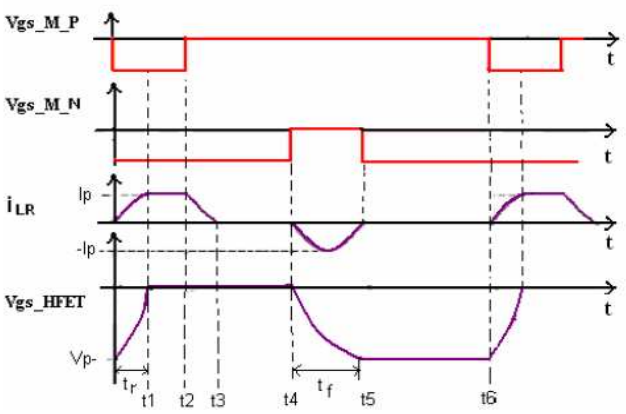

Fig. 9(b): GaN HFET Switching Waveforms

The operational sequences are as follows:

a) At t_0, when M_P turns on by negative pulse, i_{LR} begins to flow and capacitor voltage starts to develop until t_1 when current reaches peak value of I_p:

$$I_p = \frac{V_{ss}}{R_g}\frac{\pi}{2} \tag{15}$$

This charges parasitic capacitor $C_{iss.}$

b) When voltage across C_{iss} reaches value slightly higher than 0 at t_1, D_1 starts to conduct and clamps V_{gs} at 0. At this time, i_{LR} continues to freewheel along D_1.

c) At t_2, when M_P is off, i_{LR} decreases that makes D_3 turns on. This i_{LR} flows through path V_{SS}-D_3-L_R-D_1-GND and then returns back to voltage source, V_{ss} after turn on transient. D_1 and D_3 act provide low impedance path for i_{LR} and return drive energy back to voltage source after turn on transient.

d) Between t_2 and t_3, i_{LR} decreases from I_p to 0 and gate-source voltage of switch remains at 0.

e) At t_4, M_N turns on and i_{LR} starts to flow in the opposite direction discharging HFET parasitic capacitor C_{iss} until the voltage reaches maximum value at V_p- at t_5. V_p- is expressed as:

$$V_{p-} = \frac{2}{\pi}\frac{V_{ss}}{R_g}\sqrt{\frac{L_R}{C_{iss}}} + \frac{V_{ss}}{2} \tag{16}$$

At the same time, D_2 prevents opposite resonant i_{LR} from flowing and voltage V_{gs} remains at V_p- until M_P turns on at t_6. Then the same process repeats.

A. Loss Analysis of GaN HFET RGD Circuit

RGD circuit shown in Fig. 9(a) contains a LC tank which can recover part of the energy. Since the auxiliary switches dissipate little loss, power dissipation can be limited. Due to the fact that parasitic capacitance of GaN FET is small, the required inductance, L_r is also small so that parasitic inductance can be used as total inductance for LC tank itself. This saves a physical component on the board. The inductor current i_{LR} and power losses of circuit are given by:

$$iL_R(t) = \frac{2V_{ss}}{\sqrt{\frac{4L_R}{C_{iss}}}} e^{-\frac{R_g}{2L_R}t} \sin\left(\frac{\sqrt{\frac{4L_R}{C_{iss}} - R_g{}^2}}{2L_R}t\right) \tag{17}$$

$$P_{loss} = \frac{R_g}{(R_g + Z_0)} C_{iss} |V_{p-}| V_{ss} f_s \tag{18}$$

From P_{loss} in (18) above, this confirms the linear dependence of power loss from parasitic gate resistance of GaN HFET. Decreasing parasitic resistance of GaN HFET reduces power loss. Only small voltage source can be used to generate higher gate-source voltage for the switch and this function will reduce demand for level shifter and hence reduces power losses. Level shifter (using ASIC implementation) is required to change voltage level of input control signals if the threshold voltage to turn off GaN HFET greater than V_p-. The level shifter can be avoided if N and P channels MOSFET are used. In addition, this RGD circuit is tolerant of timing variation. The functions of D_1 and D_2 lower the requirement for accurate pulse width control signals which is important in high frequency speed. There exists only a small pulse width variation of control signal and this will not affect the switching and discharging processes. D_2 is preventing opposite i_{LR} from flowing during the increasing i_{LR} freewheeling time.

V. Application of RGD Circuit for High Power GaN HEMT Device

The diode-clamped RGD power MOSFET circuit is shown in Fig. 10(a) and its waveform in Fig. 10(b) [1, 5, 28]. It can be modified and applied for RGD circuit design to drive GaN HEMT switch in VHF circuit.

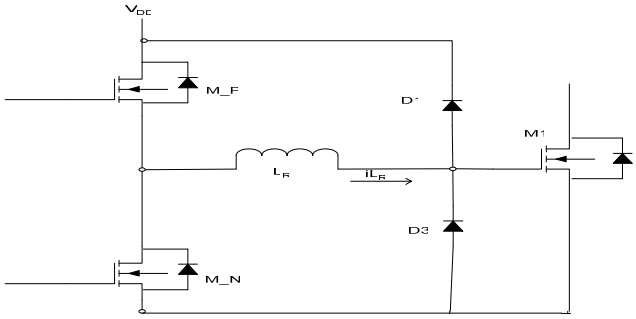

Fig. 10(a): Diode-Clamped RGD circuit

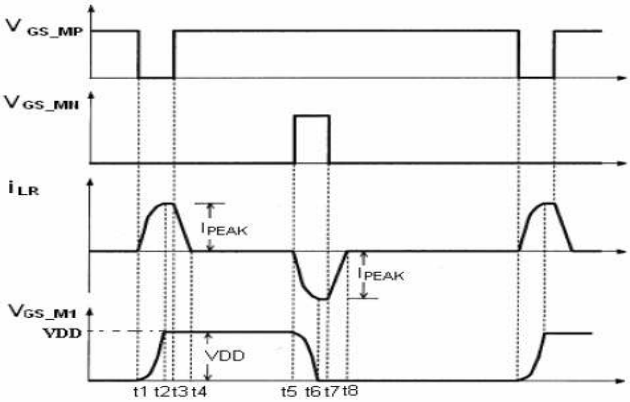

Fig. 10(b): Diode-Clamped RGD Switching Waveforms

The RGD circuit shown in Fig. 10(a) above is suitable to operate in VHF. The driving energy can be recovered fully during charging and discharging transitions. Switching losses in M_P and M_N will be reduced. The driver conduction losses are kept minimal but still needs further improvement.

This RGD circuit requires a mechanism to control the gate voltage of power MOSFET from being floating when it is in ON and OFF states. It is neither clamped to V_s nor ground by low impedance path. Consequently this allows for interference of noise which may lead to false triggering. Generally, in spite of several disadvantages, an improved RGD circuit will still need to be developed to solve these issues, thus making GaN HEMT device to operate effectively in VHF environment.

VI. Important Parameters in RGD Circuit Design

There have been debates about the issues in getting the future design of RGD circuits to be more self tolerance in noise immunity, autonomous in varying duty cycle, reduced in power dissipation as well as fast in switching speed. Either by using power MOSFET or any other improved devices from group III-V semiconductor such as GaN, SiC or GaAs, the output of the gate drive circuit must always be able to suit for VHF switching. The propagation delay or dead time between switching transitions of power MOSFET is vital in ensuring higher speed and lower conduction losses. Even though switching loss and speed are inversely proportional to each other, at least by having optimized parameters, these will result in better efficiency and reliability to the VHF RGD circuit operations.

VII. Current Work on RGD Circuit for Synchronous Buck Converter (SBC)

The proposed RGD circuit will generate two output gate voltages complementarily with a single input voltage source, V_{in} which is suitable for the SBC circuit. The operation of the circuit will utilize the symmetrical behavior of the DC-RGD. As shown in Fig. 11, the left circuit block represents the actual operation of DC-RGD circuit with optimized parameters [29]. The right circuit block, on the other hand, represents the similar circuit however the T_d between Q_3-Q_4 switches is predetermined differently. The rest of the parameters remain the same.

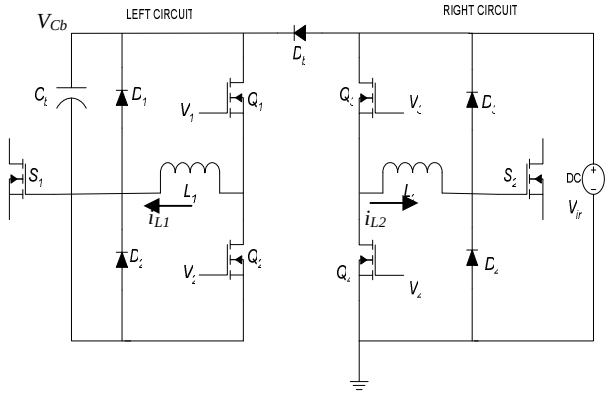

Fig. 11 Proposed RGD Circuit

There are the additional diode and capacitor, namely, D_b and C_b. They are used for high side drive in SBC being the bootstrap circuit. This circuit has the advantages in circuit simplification, symmetrical behavior and hence minimizes the switching loss. Moreover, it has better immunity in dv/dt turn-on and less impact by parasitic capacitance.

The proposed new RGD circuit consists of four switches Q_1-Q_4. Both sets of switches Q_1-Q_2 and Q_3-Q_4 behave symmetrically. The inductors, L_1 and L_2 connect the driving switches to the power MOSFETs, S_1 and S_2 which represent the high and low side switch for the SBC circuit respectively. The RGD provides two drive signals with duty cycle D and 1-D. This is suitable for driving two MOSFETs at a time. The duty cycle for S_1 is D and for S_2 is 1-D. In both high and low side configuration of the proposed RGD circuit, the independent inductor currents in L_1 and L_2 will flow through the resonant-link train that depend on the conduction of all four switches, Q_1-Q_4. Since both sets of switches operate symmetrically, the amount of effective resonance effect is approximately equal, and hence the switching loss is controllable. Fig. 12 shows the operating waveforms of the proposed RGD circuit.

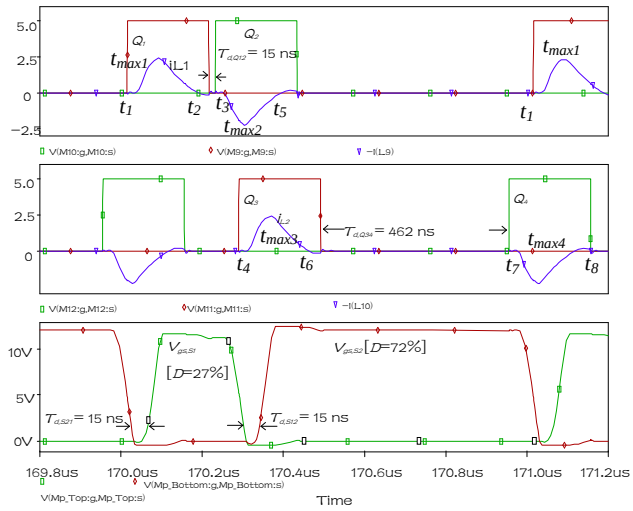

Fig. 12 Operating Waveforms of Proposed RGD Circuit

All of the switches are assumed to be initially off. At t_1, switch Q_1 starts to conduct. Here, the inductor current of L_1, i_{L1} charges to maximum at t_{max1}. Then this current will discharge through free-wheeling low impedance path, $Q_{2,bodydiode}$-L_1-D_1-V_{cb}. This discharged i_{L1} depends on the amount time given by the conduction of Q_1. In this case, the duty ratio, D of 20 % is used for the purpose. If the discharging time is insufficient, this gives rise to oscillation of the current at the end of Q_1 turn off at t_2. This result is not desirable as it leads to higher switching loss.

After a predetermined T_d of 15 ns, the switch Q_2 is then turned on. Q_1 is now turned off. Again, the i_{L1} behaves symmetrically as for the conduction of Q_1 switch. However, at t_3, i_{L1} again charges to maximum current with negative value at t_{max2}. This value is slightly lower then $iL_{1,max}$ at t_{max1} due to the leakage current during the freewheeling process. Due to the symmetrical behavior of the circuit, at t_4, Q_3 is turned on. At this time, Q_2 is still conducting while Q_4 is off. With similar fashion, the inductor current, i_{L2} is charged to maximum positive value at t_{max3}. The previous negatively i_{L1} will increase back to zero at t_5 through D_2-L_1-$Q_{1,bodydiode}$-V_{cb} as well as i_{L2} decrease to t_6 through $Q_{4,bodydiode}$-L_2-D_3-V_{in}. During the conduction of Q_1-Q_2, gate voltage of S_1, $V_{gs,S1}$ is clamped at V_{in}. For the high side SBC circuit, the duration of the conduction of $V_{gs,S1}$ is from t_1 to t_{max2} which represents D.

The process of resonant inductor current, i_{L2} is identical to i_{L1}. The rest of the operation from t_7-t_8 is the same as for t_3-t_5. The only difference is that the dead time $T_{d,Q34}$ is set to be 462 ns. This T_d value is optimized for the generation for $V_{gs,S2}$ at *1-D* from t_4 to t_{max4} and thus, makes it suitable for the low side of SBC circuit.

A. Simulation Results of Proposed RGD Circuit

The proposed RGD is evaluated in terms of total switching losses in the circuit including both S_1 and S_2 gate drive losses. Two sets of totem poled drive topologies are used incorporating bootstrap circuitry in the RGD circuit. From Fig. 11, four MOSFETs are applied to generate pulses at high and low side switches of SBC circuit. Since S_2 gate pulse is much lower than S_1, this makes total gate drive loss slightly lower in S_2. The total gate drive loss would be the summation of losses in these two switches. However, the output of SBC circuit is not influenced much by this difference.

The total RGD power losses comprise of the following distributions, namely: body diode conduction losses in the driving switches, gate resistance power losses in RGD, gate drive losses of driving switches and losses occurred in inductor, which is considered to be around 20 mW for V_{in} of 12 V. Assuming that Q_1-Q_4 are of the same type and all voltage drops, V_f of the diodes equal to 0.7 V, the distribution of the losses are formulated in equation (19) to (21).

$$P_{bdQ1,4} = 2\left(\frac{2V_f}{V_{in} + 2V_f}\right).\frac{Z_0}{R_g + Z_0} Q_{vin}.V_{in}.f_s \qquad (19)$$

$$P_{Rg} = \frac{2R_g}{R_g + Z_0} Q_{vin}.V_{in}.f_s \qquad (20)$$

$$P_{gate} = 4Q_{vin}.V_{in}.f_s \qquad (21)$$

The characteristic impedance of the resonant circuit is $Z_0 = \frac{L_{1,2}}{C_{inM1,2}}$, Q_{vin} is the gate charge of the driving switches at 12 V and switching frequency, f_s = 1 MHz. For $L_{1,2}$ and $C_{inM1,2}$ are determined to be 9 nH and 7 nF respectively, the total gate driver losses are tabulated in Table I.

TABLE I.

Proposed RGD Circuit					
V_{gs}=12 V	$P_{bdQ1,4}$	P_{Rg}	P_{gate}	$P_{inductor}$	**Ptotal**
	5 mW	125 mW	340 mW	20 mW	490 mW
	Conventional Gate Driver [30]				
	V_{gs}=12V	P_{g_chg}	$P_{\_driver}$	**Ptot_conv**	
		1.607 W	0.3 W	1.907 W	

From Table I, it indicates that the proposed RGD circuit can reduce total gate drive losses by 74 % compared with the conventional. The major contributor of losses comes from gate driving switches, P_{gate}. This is different than reported in [30] that gate resistance power losses, P_{Rg} are dominant. As P_{gate} losses are always present in the system and part of the internal structures of devices, the only way to reduce these is by reducing the number of components in the circuit. However, this is not possible. Reducing components will affect the main operation of the circuit. The proposed RGD circuit in this work is found to better leading to an improvement of 3.2 % (506 mW to 490 mW) in total gate drive losses compared to the RGD as discussed in [30].

VIII. Conclusion

In the design of VHF RGD circuit, there are limitations and drawbacks. Low conduction losses and higher switching speed are important in VHF circuits. This includes the isolation techniques to avoid mismatch and interruption of signals, the dead time delay between switches, size of components and choice of optimized parameter. Where most of RGD circuits use power MOSFET as the switching device, the newly developed high power GaN HEMT can be applied for VHF switching operation. Even though this high power GaN HEMT is not yet commercially available, the applications on RGD circuits can be realized in the near future. Studies have shown that some RGD circuit designs using power MOSFET can be modified and instead use this high power GaN HEMT device. However, the investigation on circuit performance and reliability on signal integrity have to be furthered explored due to their differences in semiconductor properties and electrical characteristics. A new proposed RGD circuit utilizing diode-clamped technique is introduced to drive synchronous buck converter circuit with low switching and conduction losses. The gate drive losses have shown improvement of 74 % compared to the conventional gate drive scheme and 3.2 % from the RGD reported in [30]. Yet, further work on isolation technique to be developed and reported on this RGD circuit.

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