A Family of DC-DC Multiplier Converters

Julio Cesar Rosas-Caro, Jonathan Carlos Mayo-Maldonado, Ruben Salas-Cabrera
Aaron Gonzalez-Rodriguez, Eduardo Nacu Salas-Cabrera, and Rodolfo Castillo-Ibarra

***Abstract*—This paper presents a topological derivation of PWM DC-DC converters by combining traditional converters with the Cockcroft–Walton voltage multiplier, the voltage multiplier of each converter is driven with the same transistor of the basic topology; this fact makes the structure of the new converters very simple and provides high-voltage gain. The traditional topologies discussed are the boost, buck-boost, Cuk and SEPIC.**

They main features of the discussed family are: *(i)* high-voltage gain without using extreme duty cycles or transformers, which allow high switching frequency and *(ii)* low voltage stress in switching devices, along with modular structures, and more output levels can be added without modifying the main circuit, which is highly desirable in some applications such as renewable energy generation systems.

It is shown how a multiplier converter can become a generalized topology and how some of the traditional converters and several state-of-the-art converters can be derived from the generalized topologies and vice-versa.

All the discussed converters were simulated, additionally experimental results are provided with an interleaved multiplier converter.

***Index Terms*— Boost converter, DC-DC power conversion, power conversion, pulse width modulated power converters.**

I. Introduction

MANI applications require a dc-dc converter with high step-up voltage gain [1-35], one of the most important applications is the green energy generation, where the low voltage from a renewable energy source need to be boosted for feeding a load or a grid connected inverter [2-6].

A very high voltage gain is difficult to achieve with traditional topologies of DC-DC converters because several reasons such as: parasitic components, the requirement of an extreme duty cycles or transformers, this limits the switching frequency and systems size [7-9]. Many topologies have been proposed to overcome those challenges with high voltage gain without the use of extreme duty cycles [1-35], with a relatively high complexity compared with the traditional single-switch converters family, the existing solutions for this challenge can be divided into several kinds such as:

Manuscript received January 14, 2011; revised January 14, 2011. This work was supported by the Dirección General de Educación Superior Tecnológica DGEST and Madero City Technological Institute in Mexico under the project MAD-MIE-2009-216 "Análisis de topologías de convertidores de potencia con alto factor de elevación para aplicación a fuentes renovables de energía".

Authors are with Madero City Technological Institute, Calle Juventino Rosas esquina con Calle J. Urueta, Ciudad Madero, Tamaulipas, CP 89440 Mexico (phone: 011-52-1-833-147-2705; rosascarojc@itcm.edu.mx).

A. Transformers or coupled-inductors based converters

Coupled inductor based converters provide solutions to achieve a high voltage gain, a low voltage stress on the active switch, and a high efficiency without the penalty of high duty ratio [2-12]. The main draw-backs are that sometimes the transformer and coupled inductor may be difficult to wind, and transformer also may introduce power losses in high frequency [13]. Two of the recently proposed converters are shown in Fig. 1, the taped-inductor boost converter proposed in [12] is shown in Fig. 1(a) while a three states commutation cells boost converter is shown in Fig. 1(b) as proposed in [6].

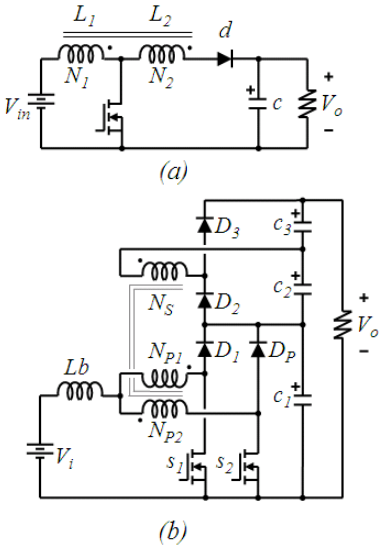

Fig. 1. Recently proposed coupled inductors based converters (a) Taped-inductor boost converter [12], (b) three-state commutation cell boost converter [6].

B. Non coupled-inductors based converters

Other important type of converters which is actually the main focus of this paper is the non coupled-inductors based converters, the research in this topic has already several decades [14-15] but there are still recently proposed and emerging topologies [13, 16-32].

Those topologies may be based on different principles of operation such as: traditional switching among inductors and capacitors [16-20], the voltage-lift technique [21-25], structures based on multipliers [26-29] and cascading converters [30]. Fig. 2(a) shows one of the step-up topologies proposed in [26] and Fig. 2(b) shows one of the step-up topologies proposed in [16].

Both topologies (Fig. 2(a) and 2(b)) charge two inductors in parallel with the input voltage and discharge them in series for getting a high step-up gain, the main draw back of those two topologies and most of high voltage gain topologies in the literature [16, 18, 19, 21-27, 30] is that the number of inductors increases again the traditional

topologies, inductors are the hardest component to build in large-scale and to encapsulate. Some of those converters are based on multiplier structures, but when they are extended to more multiplication levels, the number of inductors also increases.

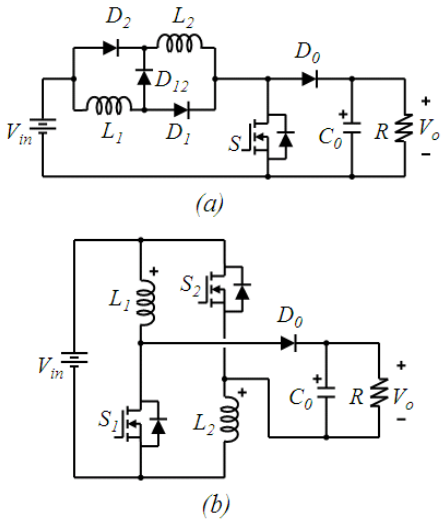

Fig. 2. (a) one of the topologies proposed in [26], (b) one of the topologies proposed in [16].

Another draw back of some topologies is that the number of driven switches increases, which increase the number of gate drives and the complexity of the converters, those switches should be synchronized and then, a control-signal mistake can damage the converter.

C. Switched-capacitor circuits

Switched capacitor converters have gain attention because of their high efficiency [32-33] but they can not regulate the output voltage by themselves, those circuits are basically inductor-less multiplier converters, their efficiency is higher than regulated dc-dc converters but as they are use for different purposes they should not be compared with dc-dc converters topologies.

Switched capacitor circuits and dc-dc converters topologies should be combined in order to get a combined higher efficiency [32-35].

The main draw back of switched capacitor circuits are high the number of driven switches and gate drives.

Since the development of high voltage-gain converters has a lot of attention, the literature is very rich, many papers has been recently published in this topic, some of the references were presented at first in a conference and then on a journal, authors decide to cite journal papers the most since they are improved and more reviewed versions. Another and more detailed classification of the different kind of converters can be found in [1] along with more references, [1] also includes a general conceptual circuit for high step-up conversion.

D. Aims of the paper

This paper extends the traditional family of PWM DC-DC converters with the Cockcroft–Walton voltage-multipliers based on diodes and capacitors; the voltage multiplier makes converters to provide a high voltage gain with several outputs of balanced voltage, this is achieved without using extreme duty cycles and transformer-lees.

Initially introduced in [39] the new family of multiplier-converters is composed so far by the boost, buck-boost, Cuk and sepic multiplier converters and derived topologies such as the three-switch high-voltage converter. Some members of the discussed family of multiplier converters have been already proposed separately in the literature [13, 21, 28-29], some of them were extended with a voltage multiplier different than the Cockcroft–Walton; other converters such as the buck-boost, SEPIC and Cuk multiplier converters are introduced in this work and they were developed following the principle of combining a traditional topology with the Cockcroft–Walton voltage-multiplier.

Generalized topologies are proposed based on the discussed topologies and it will be shown how some of the state-of-the-art topologies can be derived from the generalized topologies.

Some of the advantages of the discussed family again the state-of-the-art high voltage-gain topologies are:

(i) The proposed extension of the traditional converters doesn't increase the number of inductors in the traditional converter, inductors are bulky and hard to encapsulate, a high number of inductors decrease the power density in converters.

(ii) Each basic topology is based on one driven switch, only one gate drive is needed and as there is no synchronization between several switches, the reliability of the converter is higher compared with converters that have several synchronized switches.

(iii) The discussed family has modular structure; more output levels can be added by including diodes and capacitors without modifying the main circuit.

All the discussed converters were simulated, simulation waveforms are provided as example for the buck-boost multiplier converter, simulation and experimental results are provided for another converter which is the interleaving connection between two multiplier converters, the prototyped converter follows the general conceptual circuit for high step-up conversion introduced in [1].

I. The Multilevel Boost Converter

The first multiplier converter that will be discussed is the multiplier boost converter; this is the extension of a boost converter with a voltage multiplier. This was proposed under the name of multilevel boost converter [28-29], the name multiplier will be used for avoiding confusions with the dc-ac converter.

The first generalized structure was developed based on this converters and that is why this converter will be briefly review. Fig. 3(a) shows the traditional boost converter and Fig. 3(b) shows the *2x multiplier boost converter MBC*

A. Principle of operation

The principle of operation will be explained with the *2x extension* shown in Fig. 3(b). For analyzing this circuit an all others in this paper, the small ripple approximation [36] will be used, is assumed that the current/voltage ripple in all inductors/capacitors is small compared with their current/voltage dc component, it is considered the steady state operation of the discussed converters.

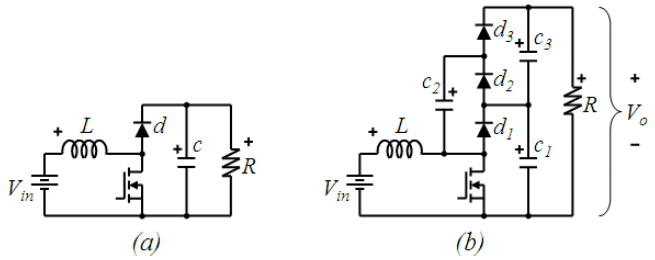

Fig. 3. (a) Traditional boost converter, (b) 2x multilevel boost converter .

When the switch is *on*, the inductor is connected to the input voltage, see Fig. 4(a), during this state the inductor is charging, when the switch is off the inductor current closes the diode d_1 (as in the traditional boost converter), and the inductor discharges, see Fig. 4(b). Fig. 4 indicates which devices are off (gray) in each switching state.

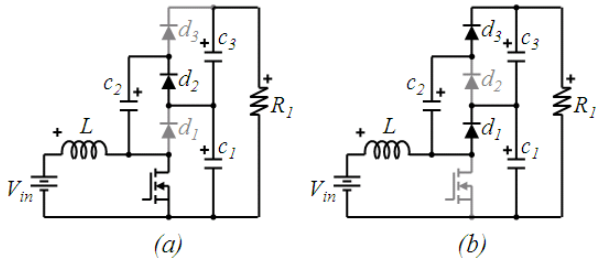

Fig. 4. Devices utilization in a *2x MBC* when the switch is on (a) and off (b).

The voltage multiplier operates in the next way: when the switch closes, the negative terminal of c_2 gets to the same point of the negative terminal of c_1, allowing c_1 to charge c_2 throw d_2, see Fig. 4(a), and when the switch opens the negative terminal of c_2 gets connected to the same point that the negative terminal of c_3 (because d_1 closes), allowing c_2 to charge c_3 throw d_3, see Fig. 4(b).

In this way, all capacitors are clamped to the same voltage, a more detailed explanation can be found in [29] along with an analysis of the voltage in each capacitor taking the diodes voltage drop into account.

B. Steady state analysis

From the equivalent circuits shown in Fig. 4, the average voltage in the inductor during one switching cycle can be expressed as:

$$\langle v_L(t)\rangle = \frac{1}{T}\left[t_{on}V_{in} + t_{off}(V_{in} - V_{C1})\right] \tag{1}$$

Where t_{on} is the time interval when the switch is on and the converter is in the switching state shown in Fig. 4(a), and t_{off} is the time interval when the switch is off and the converter is in the switching state shown in Fig. 4(b), T is the total switching period equal to $t_{on}+t_{off}$.

The first part of (1): $t_{on}V_{in}$ represents the volts per-second in the inductor during the time when the switch is *on* while the second part $t_{off}(V_{in}-V_{C1})$, represents the volts per-second in the inductor during the time when the switch is *off* and the diode is *on*. The well-known definition of duty ratio will be used to expres (1), defining the duty cycle D as the relation of t_{on} over T, (1) can be written as:

$$\langle v_L(t)\rangle = DV_{in} + (1-D)(V_{in} - V_{C1}) \tag{2}$$

Considering the operation in an equilibrium point and the volts per second balance in the inductor, this average voltage should equal zero during one switching state and then:

$$DV_{in} + (1-D)(V_{in} - V_{C1}) = 0$$
$$DV_{in} + (1-D)V_{in} - (1-D)V_{C1} = 0$$
$$V_{in} = (1-D)V_{C1}$$

$$\frac{V_{C1}}{V_{in}} = \frac{1}{1-D} \tag{3}$$

Equation (3) expresses the relation between V_{C1} and V_{in}, which is (as expected) the same relation between output and input voltage in the traditional boost converter, the interesting behavior is observed in Fig. 4, as explained the voltage multiplier makes all capacitor to charge to the same voltage V_{C1}, and the voltage multiplier can be extended with diodes and capacitors as the Cockcroft–Walton voltage multiplier.

C. Voltage multiplier extension

As shown in Fig. 5, in the same way as the AC-DC capacitor multiplier can be extended either in the positive or in the negative side, the MBC can be extended in both sides.

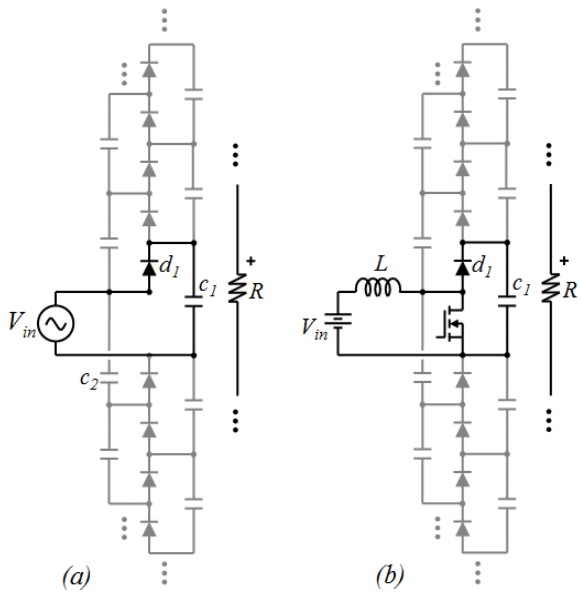

Fig. 5. (a) Cockcroft–Walton voltage multiplier (b) *Nx* multiplier boost converter.

Evidently the output voltage in Fig. 3(b) is twice of the voltage expressed in (3). The voltage-gain of the *2x multilevel boost converter* shown in Fig. 3 (b) can be expressed as:

$$\frac{V_o}{V_{in}} = \frac{2}{1-D} \tag{4}$$

The Cockcroft–Walton voltage multiplier can be extended in the same way as in the AC-DC conversion, see Fig. 5. and then, ror an *Nx* multiplier boost converter, wit *N* output capacitors, the voltage gain would be given by:

$$\frac{V_o}{V_{in}} = \frac{N}{1-D} \tag{5}$$

The capacitor multiplier in the MBC makes all capacitors

to be charged to the same voltage, even if the inductor in the boost converter is operating in discontinuous conduction mode.

II. Generalized Multiplier Boost Converter Topology

The generalized multiplier boost converter topology is shown in Fig. 6, it is similar to Fig. 5 with an optional low-pass filter (depends in the selected number of diodes). Diodes and capacitors are labeled and number as positive or negative according with their relative position to the switch.

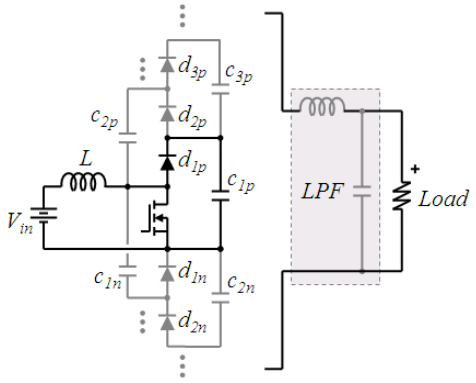

Fig. 6. Generalized multiplier boost converter topology with an optional low-pass filter.

The rules for deriving a topology from the generalized topology are:

Rule 1: *Select any number of positive and negative diodes along with their respective capacitors, and delete all diodes and capacitors over-under the more positive/negative diode we select*. Clearly if only the first positive diode d_{1p} (with its capacitor c_{1p}), the traditional boost converter would be obtained.

Rule 2: *If the load is connected among a series connection of capacitors, do not use the low-pass filter, otherwise use it*. It is important to notice that the Rule 1 allow to connect the load (with the optional low-pass filter or not) between any two points in the diode nodes, not only in the connection of series capacitors in the right side of the voltage multiplier, as proposed for the multilevel boost converter, and that is why the LPF can be necessary.

A. Deriving new converters from the generalized topology

The derivation of the boost converter or the multilevel boost converter [29] is very clear, but many other combinations of devices can be selected, for instead if we use d_{1p}, d_{2p}, d_{3p}, d_{1n} and d_{2n}, see Fig. 6, the load would be connected to the series connection of c_{2n}, c_{1p} and c_{3p}, and the low pass filter would not be necessary. Fig. 7 shows other examples of the rule.

In Fig. 7(a) the load is connected from d_{1n} to d_{2p}, among two capacitors (c_{1n} and c_{2p}) and then the LPF is not required, in Fig. 7(b) two diodes are used d_{1p} and d_{2p}, the load is connected among capacitors and diodes (c_{1p} and d_{2p}) and then the LPF is required

Under this concept, it is important to know the average voltage throw diodes, because in Fig. 7 the load voltage is given by V_{c1p} plus the average voltage in d_{2p}, the inductor and capacitor of the LPF can be easily calculated to match ripple requirements by knowing the voltage in d_{2p}, the duty cycle, input voltage and switching frequency, or it can be calculated for the worst case when the duty cycle is equal to 0.5.

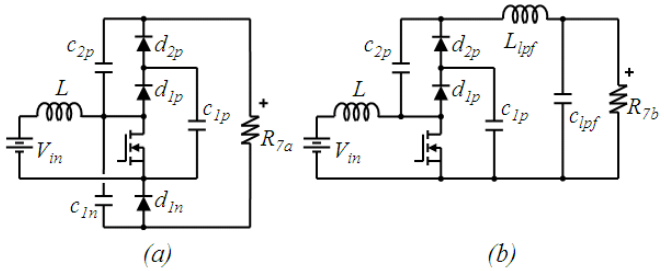

Fig. 7. Examples when (a) the low-pass filter is not required (b) the low-pass filter is required.

From Fig. 4 and the explanation of the multilevel boost converter [28-29], all pair-numbered positive diodes: d_{2p}, d_{4p}, d_{6p}, … etc. are driven synchronized with the switch, and all other positive diodes (odd-numbered): d_{1p}, d_{3p}, d_{5p}, … etc. switch complementary with the transistor.

For the negative side of the voltage multiplier extension, the rule is opposite, all pair-numbered negative diodes: d_{2n}, d_{4n}, d_{6n}, … etc. are driven synchronized with the switch, and all other negative diodes (odd-numbered): d_{1n}, d_{2n}, d_{3n}, … etc. switch complimentary with the transistor.

All diodes are connected to the same voltage when they are open, which is the voltage in capacitors, which is also the same in all of them, this is one of the advantages of the topology which follows the multilevel converters principle, the differences is that some of them are closed with the switch and then the average voltage on them would be expressed as:

$$\langle v_d \rangle = (1-D)\frac{1}{1-D}V_{in} = V_{in} \tag{6}$$

Which is the voltage in all capacitor times the compliment of the duty cycle, in the other hands diodes which are complementary with the switch, has a voltage expressed as:

$$\langle v_d' \rangle = D\frac{1}{1-D}V_{in} \tag{7}$$

Which is the voltage in all capacitors times the duty cycle.

From this analysis is easy to calculate the output voltage in the converter in Fig. 7(a) as:

$$V_{R7a} = V_{c1n} + V_{c2p} = \frac{2}{1-D}V_{in} \tag{8}$$

Because all capacitors have the voltage expressed in (3), and for the converter in Fig. 7(b) the output voltage would be given by:

$$V_{R7b} = V_{c1p} + \langle v_{d2p} \rangle = \left(\frac{1}{1-D}+1\right)V_{in}$$

$$V_{R7b} = \frac{2-D}{1-D}V_{in} \tag{9}$$

Converters shown in Fig. 7 are new, but they are only examples of specific topologies derived from the generalized topology, and they won't be deeply studied.

B. C-switching blocks converters

The *2x MBC*, see Fig. 3(b) can be fount by taking both diodes over the switch, and both capacitors over the switch along with capacitor c_1, instead of taking those diodes and capacitors is possible to take the diode under the switch d_{1n} and c_{1n}, as shown in Fig. 8 (a).

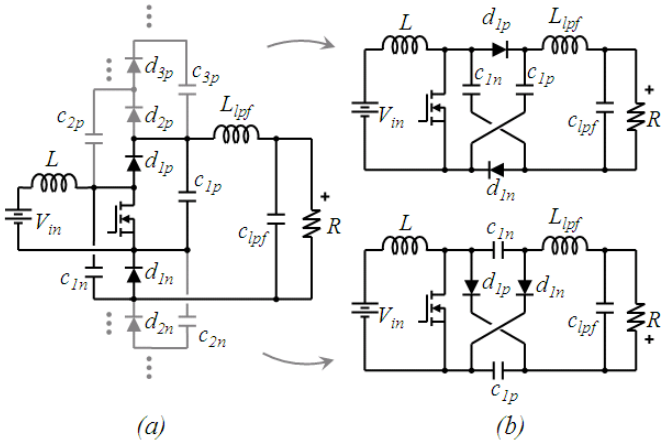

Fig. 8. (a) Generalized topology (b) two of the topologies proposed in [26].

Since the output voltage would be Vc_1 plus the voltage in d_2, which is give by (7) because is an odd-numbered diode in the negative side, the output voltage would be discontinuous, a low-pass filter can smooth the voltage as shown in Fig. 8, the voltage in the output is expressed as:

$$V_R = V_{c1p} + \langle v_{d1n} \rangle = \left(\frac{1}{1-D} + \frac{D}{1-D} \right) V_{in}$$

$$V_R = \frac{1+D}{1-D} V_{in} \qquad (10)$$

Equation (10) shows that the converter in Fig. 7(b) has a higher voltage gain than converters shown in Fig. 8(b) with the same number of components rated to the same parameters.

Converters shown in Fig. 8(b) are two of the topologies proposed in [26] as C-switching blocks converters, (same as Fig. 8 and Fig. 15 from [26]). It should be mentioned that authors of [26] got those converter following a different procedure and proposed other topologies which doesn't follow the generalized topology.

C. The Cuk converter

Another example is: if we use only d_{1n} and c_{1n}, see Fig. 9, and by connecting the load in d_{1n} (with the low-pass filter since the load would be connected among one diode) the traditional Cuk converter can be derived, see Fig. 9. As expected the load voltage would be given by (7) since that is the average voltage in all diodes which switch complementary with the transistor, as d_{1n} which is an odd-numbered negative diode.

It is important to notice that the way of connecting the low-pass filter, with the inductor in the cathode or in the anode of the diode affects neither the operation nor the output voltage.

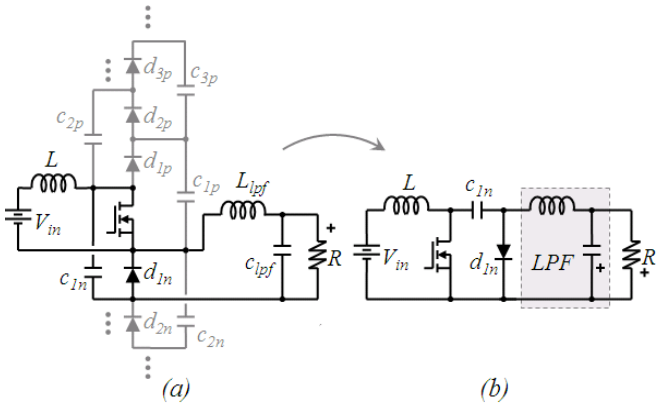

Fig. 9. (a) Generalized topology (b) Traditional Cuk converter.

D. The multiplier Cuk converter

A multiplier extension of the Cuk converter can be also obtained from the generalized topology when more negative diodes are used, if an odd number of negative diodes are used the converters keeps with the same structure of the Cuk converter, see Fig. 10.

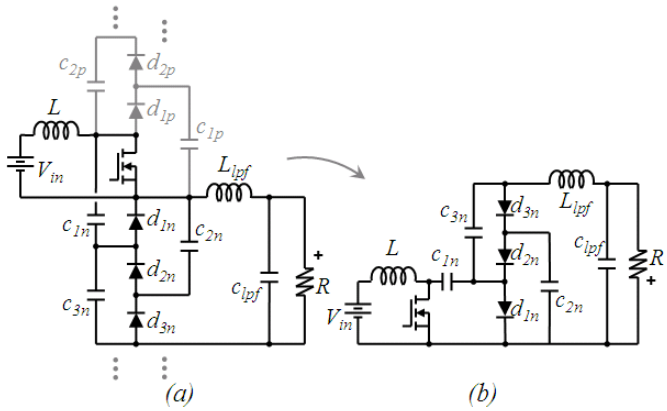

Fig. 10. (a) Generalized topology (b) 2x multiplier Cuk converter.

Following the same rule for calculating the voltage gain in the converter in Fig. 10, and considering that the average voltage in d_{3n} is expressed as (7) because it is an odd negative diode, the voltage gain of the converter in Fig. 10(b) would be expressed as:

$$V_R = V_{c2n} + \langle v_{d3n} \rangle = \left(\frac{1}{1-D} + \frac{D}{1-D} \right) V_{in}$$

$$V_{R7b} = \frac{1+D}{1-D} V_{in} \qquad (11)$$

It can be seen from Fig. 10 that the voltage multiplier can be extended in the Cuk converter and any number of capacitors (output voltage-levels) can be selected.

E. The three-switch high-voltage converter and some voltage lift converters

When a multiplier converter is derived from the generalized topology, it can be selected to use or not to use the output low-pass filter; not using the LPF saves one inductor which is desirable. If a pair-number of diodes is selected in the negative side of the generalized topology, the low pass filter can be avoided, as shown in Fig. 11.

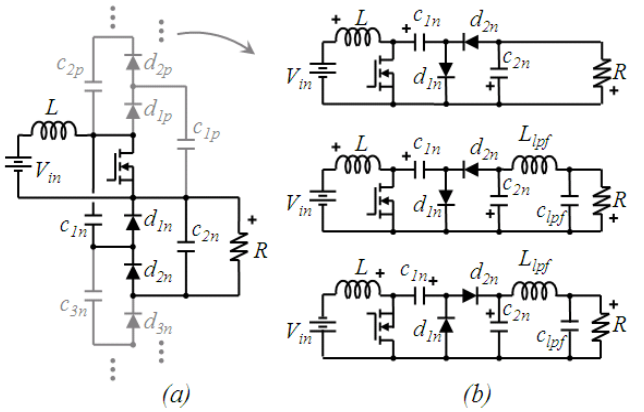

Fig. 11. (a) Generalized topology (b) from top to bottom: converters proposed in [13, 24, 21] respectively.

Fig. 11(a) shows the example of taking two negative diodes, the voltage gain is the same as the boost converter, as the load is connected to one capacitor in the voltage multiplier, Fig. 11(b) shows several converters proposed with this structure.

In [13] the converter was proposed as a three-switch high-voltage converter (see Fig. 2(a) in 13). The extension of authors proposed for this converter follow the generalized topology by taking more negative diodes in pair-number, and then no low-pass filter is required.

In [24] the output low-pass filter was used, see Fig. 11(b) in the middle this was proposed as a voltage-lift-type cuk converter, the low-pass filter is optional because c_{2n} can be calculated large enough to maintain a constant voltage with a small ripple (see Fig. 2(a) in [24]). In this case the voltage multiplier was extended with a different way (not the Cockcroft–Walton voltage-multiplier) but with the voltage-lift technique and then the extension of the converters doesn't follow the generalized topology, only the firs level extension follow the generalized topology.

In [21] a converter was proposed for negative to positive voltage conversion with the structure in Fig. 11(b) in the bottom, as in all dc-dc unidirectional converters, by inverting all diodes and switch, and the polarity of the input voltage, a polarity change in the output voltage can be achiever (see Fig. 1 in [21]). In this case an extension of the converter was not proposed but it can be achieved by extending the Cockcroft–Walton voltage-multiplier or the voltage-lift technique as developed in [24].

F. *Another similar converter*

In [27] authors proposed hybrid structures of traditional converters with another kind of voltage multiplier cell. Fig 12 shows the boost converter with one multiplier cell (same as Fig. 3(b) in [27]), as authors in [27] mentioned, the topology can work without the inductor L_r which is not for energy storage but only for resonance purposes, furthermore, the output capacitor has twice of the voltage to C_{M1} in Fig. 12(a) because of the multiplier cell, then it can be represented as two capacitors in series with the same voltage, see Fig. 12, C_{o2} has the same voltage of C_{M1}, and then they can get in parallel connection.

Authors in [27] present a similar topology of Fig. 12(b) for getting symmetrical output voltage, and they extend the topology for more getting a higher multiplication factor, but for extending the multiplication factor they connect more cascaded multiplication instead of extending it as a Cockcroft–Walton voltage multiplier and then, the extension of the multiplication factor doesn't follow the generalized topology.

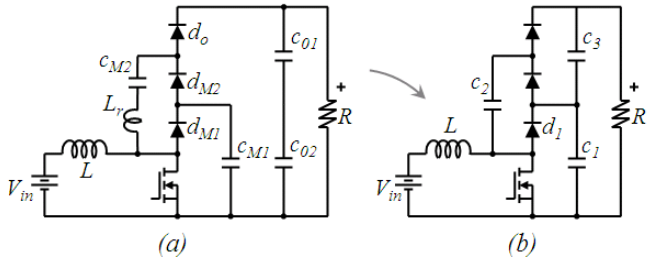

Fig. 12 (a) First structure proposed in [27] (b) *2x MBC*.

III. Other Multiplier Converters

In the same way as the traditional boost converter can by combined with the Cockcroft–Walton voltage-multiplier, which was the procedure for obtaining the multilevel boost converter that became the generalized topology explained in section II, other traditional converters can get this kind of hybrid structures such as the.

A. *Multiplier Cuk converter*

This converter can be derived from the generalized topology as shown in the past section, but the extension of the multiplier structure can be in the negative side, as shown in Fig. 10, or in the positive side as shown in Fig.13. The generalized structure for getting a multiplier Cuk converter with any number of levels can be seen in Fig. 13(b).

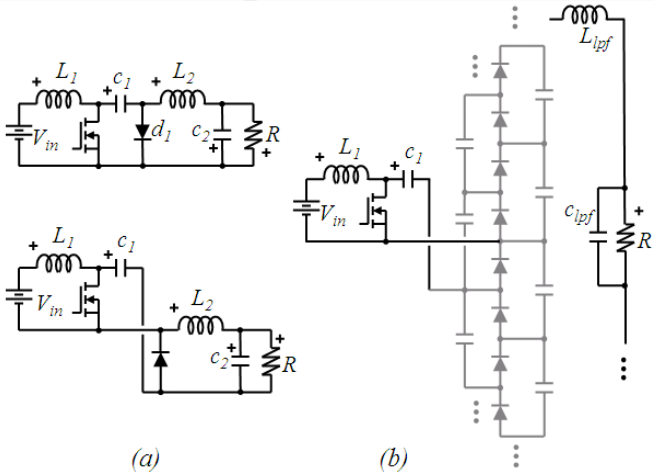

Fig. 13 (a) Traditional Cuk converter (b) Multiplier Cuk converter.

B. *Multiplier Buck-Boost converter*

Fig. 14(a) shows the traditional buck-boost converter; Fig. 14(b) shows the 2x *multiplier buck-boost converter MBBC*, which is the natural extension of the traditional buck-boost converter with the Cockcroft–Walton voltage-multiplier, and Fig. 14(c) shows the generalized topology for getting a buck-boost multiplier converter with any number of diodes and capacitor in the voltage multiplier.

The multiplier buck-boost converter is a new topology, it can not be derived from the generalized topology shown in Fig. 6 and then it will be analyzed with more detail than the other topologies.

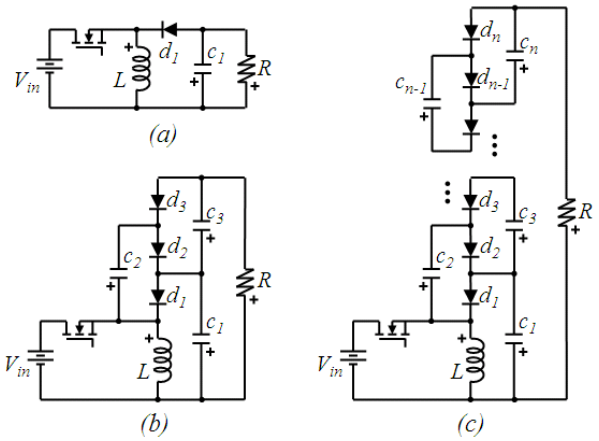

Fig. 13 (a) Traditional buck-boost Converter (b) *2x* multiplier buck-boost converter (c) *nx* multiplier buck-boost converter.

The *2x* multiplier buck-boost converter will be used for analyzing the topology, Fig. 14(a) and Fig. 14(b) show the devices utilization when the switch is on and off respectively.

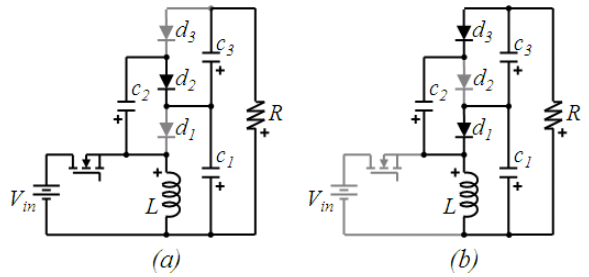

Fig. 14 *2x* multiplier buck-boost Converter (a) when the switch is on (c) when the switch is off.

As in the traditional when switch turns off, the inductor current closes d_1, allowing c_2 charging c_3 throw d_3, and when the switch turns on, V_{in} and c_1 charge c_2 throw d_2.

Assuming the small ripple approximation and the duty cycle defined in the previus analysis, $D=t_{on}/T$, the average voltage in the inductor during one switching cycle, can be expressed as:

$$\langle v_L(t)\rangle = DV_{in} - (1-D)V_{C1} \tag{12}$$

Considering the operation in steady state, this voltage should be equal zero and then:

$$DV_{in} - (1-D)V_{C1} = 0$$
$$DV_{in} = (1-D)V_{C1}$$
$$\frac{V_{C1}}{V_{in}} = \frac{D}{1-D} \tag{13}$$

The voltage in c_1 is as expected the same as in the conventional buck-boost converter, the voltage multiplier in this case charge c_2 with $V_{in}+V_{C1}$ throw d_2 when the switch is on, see Fig. 14(a), and it charges c_3 with V_{C2} throw d_3 when the switch is off, see Fig. 13(b). In steady state operation the voltage in both capacitors c_2 and c_3 with the small ripple approximation can be expressed as:

$$V_{C2} = V_{C3} = V_{in}\left(1+\frac{D}{1-D}\right) = V_{in}\frac{1}{1-D} \tag{14}$$

And finally the voltage in the output resistor in Fig. 13(b) is the sum of V_{C1} and V_{C3}, and it can be expressed as:

$$V_R = V_{in}\left(\frac{1}{1-D}+\frac{D}{1-D}\right) = V_{in}\frac{1+D}{1-D} \tag{15}$$

The MBBC has a behavior more similar to the conventional capacitor multiplier, see Fig. 5(a) where c_1 and c_2 are charged to the input voltage while all other capacitors are charged to twice of the input voltage. In the MBBC c_1 is charged to the voltage expressed in (5) while c_2 and c_3 are charged to the voltage expressed in (6) which is higher, see Fig. 4 where the voltage in c_1, all other capacitors, the output voltage in the *2x* MBBC and the output voltage in the *2x* MBC (only for comparison purposes.

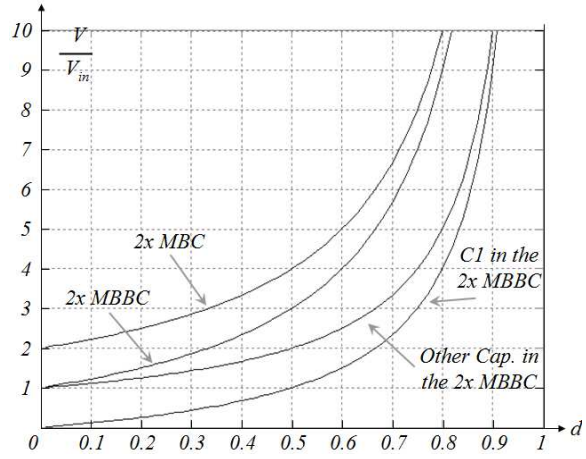

Fig. 15. Voltages again duty cycle.

Increasing the switching frequency of the converter is easier when the converter is designed for working with a duty cycle D around 0.5, this converter as other multiplier converters discussed in this paper can be designed to work with a duty ratio around 0.5, the voltage multiplier can be used to select the voltage gain desired when the duty cycle is near 0.5.

Fig. 13(c) shows the multilevel extension of the buck-boost converter in the negative side, but the diode-capacitor multiplier can be extended in the positive side too. Fig. 16 shows the diode-capacitor multiplier extension in both sides. As it can be seen from the analysis, capacitors c_{1n} and c_{1p} in Fig. 16(b) has a voltage gain given by (13) and all other capacitors in Fig. 16(b) have a voltage given by (14).

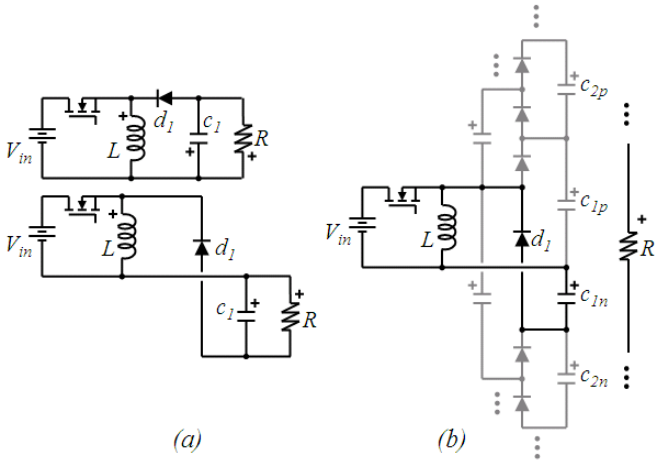

Fig. 16. (a) traditional buck-boost converter (b) generalized buck-boost converter multiplier converter topology.

C. Multiplier SEPIC converter

Fig. 11 shows the multiplier SEPIC converter as the combination of the traditional SEPIC converter with the Cockcroft–Walton voltage-multiplier, this is another topology which can not be derived from the generalized topology but the same analysis can be developed.

The key-point of deriving a multiplier converter is that all traditional converters share a basic behavior; they have a diode which is open and closed by the converters operation, this diode is turning off by a reverse bias voltage which can be used to charge another capacitor throw a diode, and in this way start a diode-capacitor multiplier.

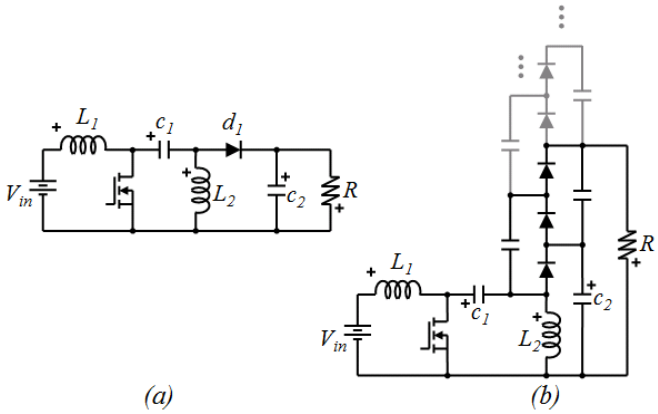

Fig. 17. (a) traditional SEPIC converter (b) multiplier SEPIC conerter.

At least one multiplier converter has been proposed in recent literature [22], but it uses a different principle and the multiplier extension is not based on the Cockcroft–Walton voltage-multiplier, but in the voltage lift technique.

IV. Interleaving Multiplier Converters

Interleaved converters provide several improvements again traditional converters such as small-size inductors with low current ripple in the input voltage (for converters with the capability of boosting the voltage), and better dynamic behavior since inductors are smaller, they can change their current in a shorter time.

Multiplier converters can be also connected in a interleaving way, and the input current can be canceled (in multiplier converters with an input inductor).

And advantage of the discussed converters is that the number of inductors is not increased with the voltage multiplier, if two converters are interleaved then at least two inductors are needed but they are smaller and then the size doesn't increase, as in traditional interleaved converters.

A. Interleaving positive output multiplier converters

Fig. 17 shows the interleaved connection of two *2x* multiplier boost converters, both converters share capacitors in the output.

Some renewable energy sources require a very small output current-ripple, which is given by the converter connected in the output, a converter with small input current-ripple is highly desirable, the converter in Fig. 17 can provide this characteristic with small inductance in both inductors.

The voltage gain keeps the same as in the *2x* multiplier boost converter, the advantage is the reduced input current and the small size of inductors (the ripple current in each inductor is higher but they cancel each other).

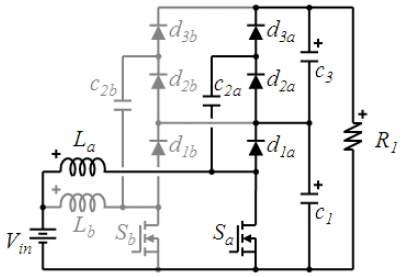

Fig. 17. Interleaved 2x multiplier boost converter.

B. Interleaving a positive output with a negative output multiplier converter

The best way of interleaving multiplier converters is by interleaving a positive output with a negative output converter, in this way, the advantages of small inductors and reduced input current ripple holds while the voltage gain is higher. For this section, a topology is proposed.

Fig. 18 depicts the proposed topology, it consist in two inductors, two switches, seven diodes and seven capacitors, the input has a low ripple even with small inductors, the voltage gain is high and can be extended with a diode-capacitor multiplier, it provides multiple outputs in the series connected capacitors with self voltage balance, ideal to feed a diode clamped multilevel inverter.

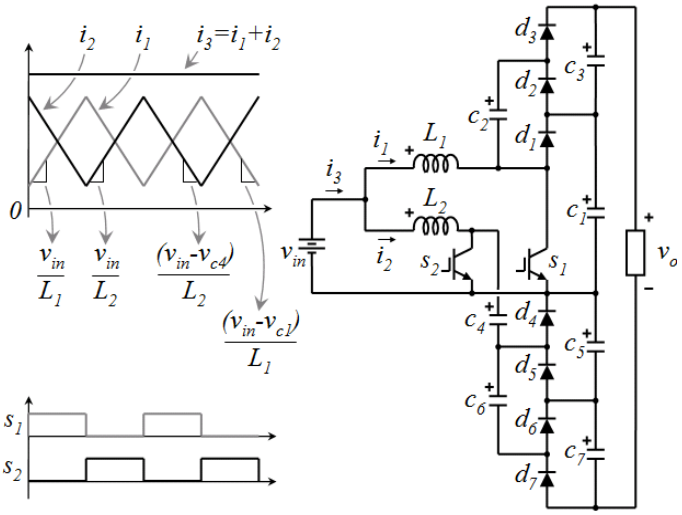

Fig. 18. Proposed interleaved multiplier topology and important waveforms.

The proposed topology can be studied in two parts, the positive side which is conformed by s_1, L_1, c_1, c_2, c_3, d_1, d_2 and d_3 and the negative side conformed by s_2, L_2, c_4, c_5, c_6, c_7, d_4, d_5, d_6 and d_7.

C. Positive side analysis

The positive side analysis can be summarized as: When switch s_1 is closed, the inductor L_1 is connected to the input voltage and its current raises with a slope equal to the input voltage over the inductance, see Fig. 19(a).

When the switch s_1 is off, the inductance current closes d_1 as in a traditional boost converter and the inductor current decreases with a slope equal to the input voltage minus c_1 voltage over the inductance L_1, see Fig. 19(b), when the switch is closed, the negative terminals of capacitors c_1 and

c_2 are connected together allowing c_1 to charge c_2 by closing d_2, see Fig. 19(a).

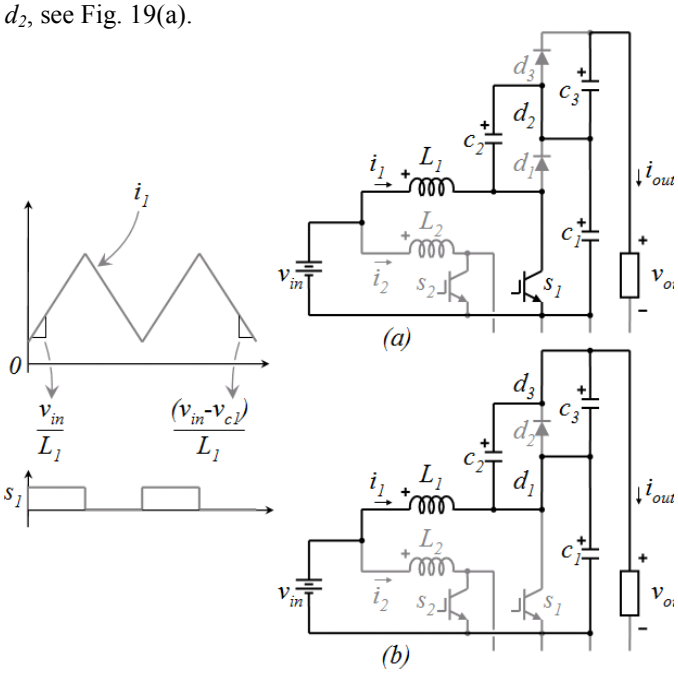

Fig. 19. Equivalent circuits of the positive side (a) when s1 is closed (b) when s1 is open.

By using the small ripple approximation [36] the average voltage in the inductor can be expressed as:

$$L_1 \frac{d\langle i_{L1}\rangle}{dt} = \langle v_{L1}\rangle = D_1 v_{in} + D_1'(v_{in} - v_{C1}) \tag{16}$$

Where D_1 is the duty cycle of switch s_1 defined as the time the switch keeps closed over the total switching period, and D_1' is defined as the complement of the duty cycle and it is equal to 1-D_1. In steady state, this voltage should be equal zero and then:

$$\begin{aligned} &D_1 v_{in} + D_1'(v_{in} - v_{C1}) = 0 \\ &D_1 v_{in} + (1 - D_1) v_{in} - (1 - D_1) v_{C1} = 0 \\ &v_{in} - (1 - D_1) v_{C1} = 0 \end{aligned} \tag{17}$$

And from (17) the voltage in c_1 can be expressed as:

$$v_{C1} = v_{in} \frac{1}{1 - D_1} \tag{18}$$

Which is the boost factor in the traditional boost converter, during the time when the switch s_1 is closed, c_2 is charged by c_1 throw d_2 and it gets the same voltage, see Fig. 19(a), during the time when the switch s_1 is open, c_3 is charged by c_2 throw d_3 and it gets the same voltage, see Fig. 19(b), and voltage in capacitors c_1, c_2 and c_3 can be expressed as:

$$v_{C1} = v_{C2} = v_{C3} = v_{in} \frac{1}{1 - D_1} \tag{19}$$

D. Negative side analysis

The negative side analysis can be summarized as: When switch s_2 is closed, the inductor L_2 is connected to the input voltage and its current raises with a slope equal to the input voltage over L_2, see Fig. 20(a), when the switch s_2 is off, the inductance current closes d_4 charging c_4.

When the switch s_2 is open the inductor current decreases with a slope equal to the input voltage minus c_4 voltage over L_2, see Fig. 20(b), when the switch is closed, the positive side of capacitors c_4 and c_5 are connected together allowing c_4 to charge c_5 by closing d_5, see Fig. 20(a).

By using the small ripple approximation [36] the average voltage in the inductor can be expressed as:

$$L_2 \frac{d\langle i_{L2}\rangle}{dt} = \langle v_{L2}\rangle = D_2 v_{in} + D_2'(v_{in} - v_{C4}) \tag{20}$$

Where D_2 is the duty cycle of switch s_2 defined as the time the switch keeps closed over the total switching period, and D_2' is defined as the complement of the duty cycle and it is equal to 1-D_2. In steady state, this voltage should be equal zero and then:

$$\begin{aligned} &D_2 v_{in} + D_2'(v_{in} - v_{C4}) = 0 \\ &D_2 v_{in} + (1 - D_2) v_{in} - (1 - D_2) v_{C4} = 0 \\ &v_{in} - (1 - D_2) v_{C4} = 0 \end{aligned} \tag{21}$$

And from (21) the voltage in c_4 can be expressed as:

$$v_{C4} = v_{in} \frac{1}{1 - D_2} \tag{22}$$

Which is also the boost factor in the traditional boost converter, during the time when the switch s_2 is closed, c_5 is charged by c_4 throw d_5 and s_2, and it gets the same voltage, see Fig. 20(a).

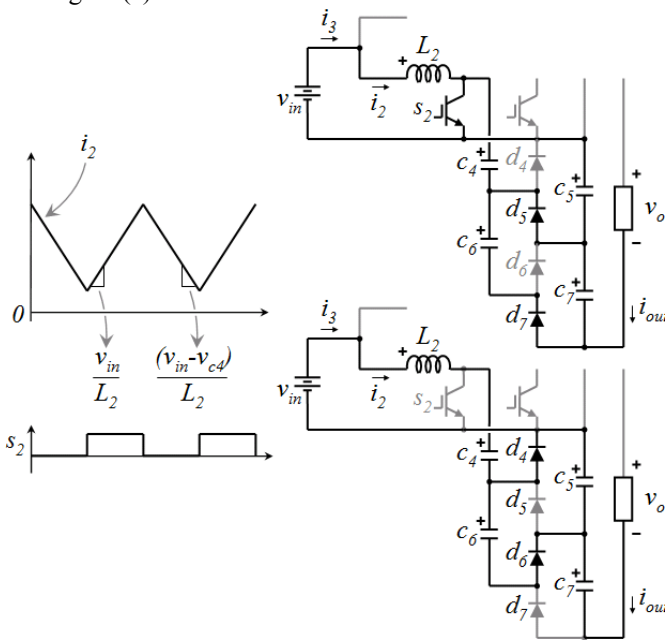

Fig. 20. Equivalent circuits of the negative side (a) when s2 is closed (b) when s2 is open.

During the time when the switch s_2 is open, c_6 is charged by c_5 throw d_6 and it gets the same voltage, see Fig. 20(b), and finally, when the switch is closed, c_7 is charged by c_6 throw d_7 and it gets the same voltage, the voltage in capacitors c_4, c_5, c_6 and c_7 can be expressed as:

$$v_{C4} = v_{C5} = v_{C6} = v_{C7} = v_{in} \frac{1}{1 - D_2} \tag{23}$$

Since the output is connected to capacitors c_1, c_3, c_5 and c_7

and assuming both switches have the same duty cycle $D=D_1=D_2$ (because of the interleaving operation) the voltage gain can be expressed as:

$$\frac{v_{out}}{v_{in}} = \frac{4}{1-D} \tag{24}$$

E. Interleaving operation

The positive side of the analysis is actually a 2x multiplier boost converter, as shown in Fig. 3(b) and [29], and the negative side of the converter is a quadrupler extension of the three-switch high voltage converter, proposed in [13], as shown in section II both of them can be derived from the generalized topology shown in Fig. 6.

As in the traditional interleaving pulse width modulation control, the PWM is based on two carriers, two comparators and one reference signal (for duty cycle), one carrier for each switch, both carriers are triangular waveforms shifted 180 degrees for providing the interleaving operation, when the duty cycle is 0.5 (the ref signal is 0.5), the current in both inductors cancel each other, see Fig 18.

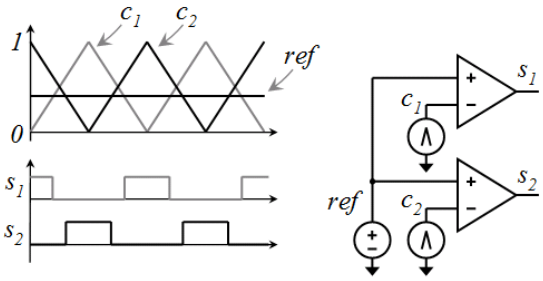

Fig. 21. Interleaved PWM scheme.

The interleaving operation provides a low input current-ripple with small inductors, highly desired in renewable energy generation systems.

The interleaved topology also follows the general conceptual circuit for high step-up conversion proposed in [1].

V. Experimental Results

The circuit in Fig. 18 was simulated and prototyped with: an input voltage of 48V, duty cycle 0.55, resistive load 985Ω, both inductors are 400µH, and all capacitors are 220µF.

Fig. 22 shows the experimental results compared with the simulation results, simulation results are shown with narrow lines. The recorded waveforms are voltage across switch 1 both inductor currents and the output voltage, all waveforms match the analysis done.

The current in experimental results seems a little delayed due the delay in the current probe.

It can be seen that the current ripple in both inductors is very high they are working almost in discontinuous conduction mode, but the ripple cancel each other because the phase shift in the switches firing signal.

This topology can feed a diode-clamped multilevel inverter to inject the generated power into the grid of feeding an AC load, the converter provides a self-balancing in the dc-link of the diode-clamped converter making the control simpler without external balancing circuits.

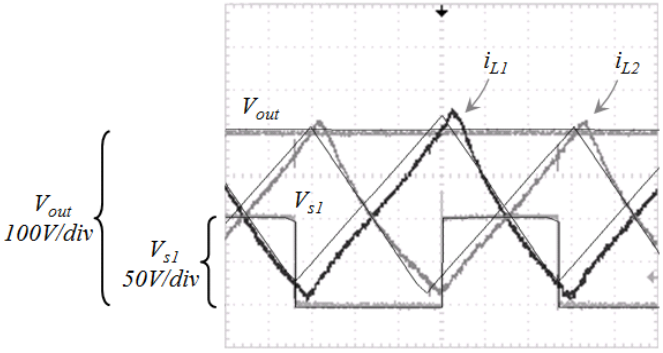

Fig. 22. Experimental results, inductors current, switch and output voltage.

Some works in the literature has proposed the use of multiplier converters to feed a diode clamped multilevel converter for renewable energy generation systems [37-38].

VI. Conclusion

This paper extends the traditional family of PWM DC-DC converters as a family of voltage multiplier converters by combining traditional converters such as the boost, buck-boost, Cuk and SEPIC with the Cockcroft–Walton voltage-multiplier; the voltage multiplier makes converters to provide high a voltage gain with several outputs of balanced voltage, this is achieved without using extreme duty cycles and transformer-lees.

Generalized topologies were proposed and it was shown how some known converters can be derived from the generalized multiplier boost converter topology, some other converters in the discussed family are introduced in this work by following the principle of combining a traditional topology with the Cockcroft–Walton voltage-multiplier.

Some of the advantages of the discussed family again the state-of-the-art high voltage-gain topologies are:

(i) The proposed extension of the traditional converters doesn't increase the number of inductors in the traditional converter, inductors are bulky and hard to encapsulate, a high number of inductors decrease the power density in converters.

(ii) Each basic topology is based on one driven switch, only one gate drive is needed and as there is no synchronization between several switches, the reliability of the converter is higher compared with converters that have several synchronized switches.

(iii) The discussed family has modular structure; more output levels can be added by including diodes and capacitors without modifying the main circuit.

All the discussed converters were simulated, simulation waveforms are provided as example for the buck-boost multiplier converter, simulation and experimental results are provided for another converter which is the interleaving connection between two multiplier converters, the prototyped converter follows the general conceptual circuit for high step-up conversion introduced in [1].

The key of deriving a multiplier converter is that All analyzed converters share a basic behavior; all of them have a diode which is open and closed by the converters operation, this diode is turning off by a reverse bias voltage which can be used to charge another capacitor throw a diode, and in this way start a diode-capacitor multiplier.

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