All Digital Time-to-Digital Converter with High Resolution and Wide Detect Range

Hong-Yi Huang, Wei-Chung Hung, Hui-Wen Cheng and Ching-Hsing Lu

Abstract—A high-resolution and wide-range all digital time-to-digital convertor is proposed in this paper. The circuit utilized a single-stage vernier delay line (VDL) with dual delay lock loop (DLL), combining with two reference clock to adjust and ensure the delay of the delay element. Several advantages can be achieved by using all digital technique, such as smaller core size, higher linearity, higher resolution and faster locking speed. The proposed architecture is implemented using 0.18 um CMOS process with a resolution between 10~80.4 ps and an input range under 162 ns. Reference clock is limited between 225~316 MHz, due to the lock-in range of the DLL. The chip area is 0.806 × 0.712 mm2 with the core area of 0.309 × 0.205 mm2. The dynamic power dissipation is 9.34 mW, and the stable power dissipation is 5.55 mW.

***Keywords*—time to digital converter, delay locked loop, Vernier delay line**

I. Introduction

TIME-TO-DIGITAL converter (TDC) is an important block that has often been integrated in mixed signal IC designs and precise instrument systems, such as ultrasonic flow meters and particle identification [1]-[2]; the success or failure of the system mainly depends on the accuracy and converting time of TDC. Although using VDL technique [3] can achieve high accuracy, there remains space for improvement. Higher accuracy accompanies slower converting time and longer delay line. However, using analog structure with voltage control delay element might result in lack of tunable range due to the steep slope of the bias voltage versus delay time which makes a harder task of increasing the resolution to a higher accuracy. Under this consideration and pursuing the advantage of smaller area, lower power, and the possibility of process scaling down [4], digital delay lock-loop (DLL) is used to replace the analog PLL. Since the calibrating function has been modified, the ring oscillator structure must be changed. Therefore, the oscillation period of the oscillator changes synchronously, leading to an uncertainty of oscillation period in designing and measuring, interferes the accuracy of the design.

Improvements are carried out in this schematic by using delay elements calibrated by the DLL to form the oscillator, so that every element in the oscillator is controlled by the PLL/DLL. The motivation of this work is to develop a time-to-digital converter based on single-stage Vernier delay line technique with higher resolution and linearity, accompany with ultra low-power consumption and core area.

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II. Operation Principles

Fig. 1 is the block diagram of the proposed TDC with self calibration faculty. The unique part of the proposed TDC is the use of replicas delay elements in DLL of the ones in digital control oscillators (DCO) to ensure the delay elements in the oscillator has the same delay time as in the DLL. Two delay-lock loops DLL_C and DLL_F are used to stabilize and calibrate the oscillation frequencies of the two oscillators in the DCO by exploiting the reference clock and adjusting the loading of the delay element. DCO_C is adjusted by DLL_C, and DCO_F is adjusted by DLL_F. DLL_C and DLL_F use different reference clock to achieve two different time resolutions. For example, inserting a reference clock T_1 with lower frequency to DLL_C, while giving DLL_F a higher frequency T_2 makes the previous delay larger than the latter.

In the proposed TDC, reference clock is imported before the measurement signal to calibrate the oscillation period of the DCO, after the DLL locks at a certain delay time, enable signal is thus applied. When *START* signal arrives and triggers DCO_C to initiate oscillating, coarse tune counter (CNT_C) starts counting the number of oscillation period T_C of DCO_C between the rising edge of *START* and *STOP* signal. When *STOP* signal arrives, CNT_C is cut off immediately. The duration T_{coarse} shown in Fig. 2 measured by CNT_C is defined as the coarse measurement part of the operation. After the arrival of the *STOP* signal, DCO_F activates and fine tune counter (CNT_F) starts counting until the rising edge of DCO_F catches up with the rising edge of DCO_C. When two rising edge coincidence, phase coincidence detector issues an ending signal to stop CNT_F from counting; after both counter have been prohibited, the measurement ends. The remaining phase difference of *START* and *STOP* signal measured by CNT_F, shown as T_{fine}, is defined as the fine measurement part of the operation. Important issues should be noticed in CNT_F; due to the phase coincidence detector motivating at rising edge, CNT_F is triggered at least once, so the minimum output of CNT_F is one instead of zero, thus CNT_F should be measured as N_F-1 instead of N_F.

The following subsections describe the circuits of the major blocks in detail.

A. Delay Element

The proposed digital control delay element is shown in Fig. 3, with a NAND gate mounting five paralleled PMOS at the output as loading capacitor. The size of the PMOS is designed

in binary weighting, so the total delay is shown as:

$$\tau_C = \tau_{NAND} + \tau_{PMOS} \times N \quad (1)$$

where τ_C is the total delay time, τ_{NAND} is the NAND gate delay time, τ_{PMOS} is the PMOS load unit delay time, and N is the decimal of the control code A [4:0]. τ_{PMOS}×N acts as a calibrate faculty to control τ_C at a fixed delay time, hence utilizes the control code A [4:0], the delay element can be adjusted to a certain delay time.

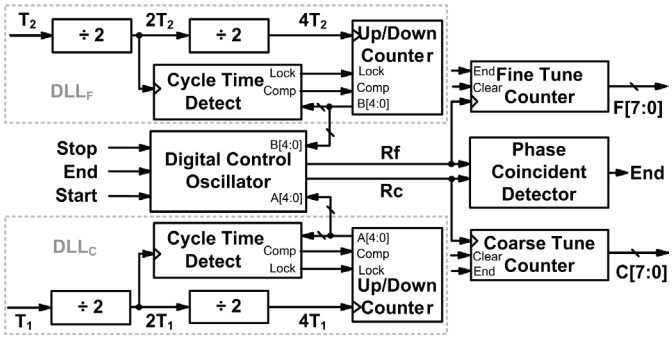

Fig. 1 Modified circuit of the proposed TDC

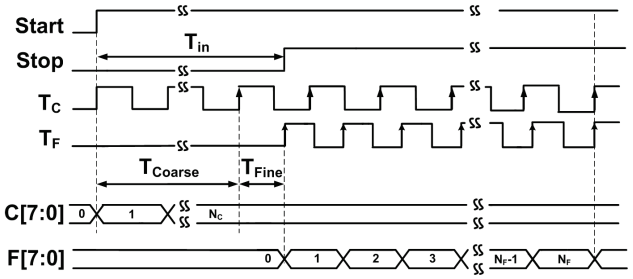

Fig. 2 Time diagram of the proposed TDC

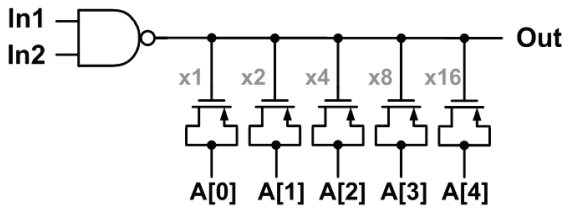

Fig. 3 Digital control delay element

B. All Digital Delay Lock Loop

The delay lock loop shown in Fig. 1 utilizes the self-calibrate function to adjust the delay element shown in Fig. 3 [5]. The purpose of cycle time detector (CTD) shown in Fig. 4 is to decompose reference clock into 32 equal divisions, assigning $\tau_C = T_1/32$. T_1 is first divided into $2T_1$ and $4T_1$ by the divider before entering DLL. The signal $2T_1$ is further sent into the delay line, which consists 33 stages of delay elements, so the positive and negative edges are both T_1. The signal is detected every time it passes the CTD, with a delay of τ_C in each stage. As shown in Fig. 5(a), if all 33 stage of the delay chain has a leading phase time compared to the negative edge of T_1, Q [33:0] is set to 1, which represents $\tau_C < T_1/32$. Therefore the 5-bit up/down counter counts up at a frequency of $4T_1$ and causes an increase of delay. However, if the counter over-counts, results of $\tau_C > T_1/32$, as shown in Fig. 5(c), the counter will start counting down. Fig. 5(b) shows the lock-in diagram of the CTD, where Q_{32} is 1 and Q_{33} is 0, therefore Lock signal rises to 1 and prohibits the counter from counting, ensuring each delay element under the control of A [4:0] a delay time of T1/32. Hence the reference period is $\tau_C = \frac{T_1}{32}$ and $\tau_F = \frac{T_2}{32}$.

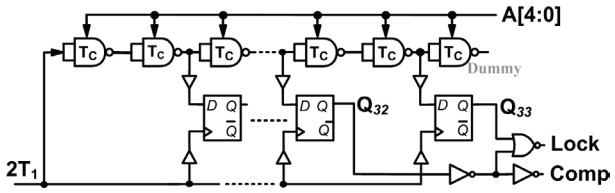

Fig. 4 Circuit of the cyclic time detector

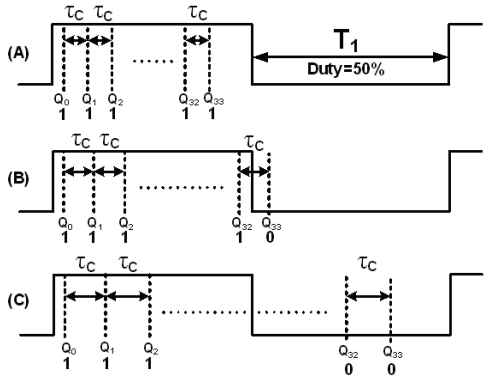

Fig. 5 Cyclic time detector lock-in diagram

C. Digital Controlled Oscillator

The digital controlled oscillator (DCO) is the major part of the circuit, directly affecting the accuracy and linearity of the TDC. In this case, special care should be taken in the design and layout. Considering the oscillation period and matching, we choose to use the delay element calibrated by the DLL to form the 5-stage ring oscillator. The proposed DCO is plotted in Fig. 6, where A [4:0] is the delay code controlled by T_1, and B[4:0] is controlled by T_2. From $\tau_C = \frac{T_1}{N}$ and $\tau_F = \frac{T_2}{N}$ we calculate the resolution of coarse resolution T_C and fine resolution ΔT, which is shown as:

$$T_C = 2 \times 5 \times \frac{T_1}{32} \quad (2)$$

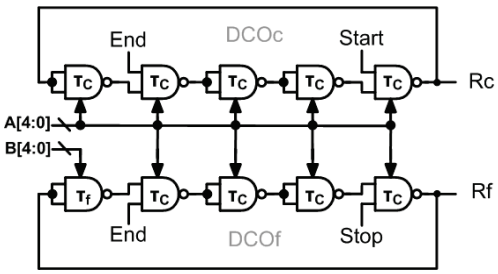

Fig. 6 Proposed digital control oscillator circuit

$$\begin{aligned}\Delta T &= 2 \times [(\tau_{CDE1} - \tau_{FDE1}) + ... + (\tau_{CDE5} - \tau_{FDE5})] \\ &= 2 \times [(\tau_C - \tau_F) + (\tau_C - \tau_C) + ... + (\tau_C - \tau_C)] \\ &= 2 \times (\tau_C - \tau_F) = 2 \times (\frac{T_1 - T_2}{32})\end{aligned} \quad (3)$$

Where τ_{CDEN} is the N_{th} delay element in DCO_C, and τ_{FDEN} is the Nth delay element in DCO_F. Only one of the delay

elements in DCO_F is controlled by B[4:0]. This modification is made to improve the fine resolution of the TDC by allowing the oscillation period of two oscillators to operate at the least possible time difference.

From Eqs. (2) and (3), the ratio of T_C and ΔT is calculated as

$$\frac{T_C}{\Delta T} = \frac{5T_1}{T_1 - T_2} \tag{4}$$

As shown in Eq. (4), the ratio and resolution of the coarse and fine measurement are controlled by the reference clock. This conception realizes within the lock-in time of the DLL.

D. Phase Coincedence Detector

The proposed PCD is shown in Fig. 7, which is divided into three stages: sampling stage, phase determining stage and output stage.

The sampling stage of the PCD uses one clock signal to sample the other, and the phase determining stage detects the state of the sampling stage. If R_c and R_f signal are phase coincidence, the output signal of phase determining stage will toggle from 0 to 1, and thus the output stage will be issued to 1.

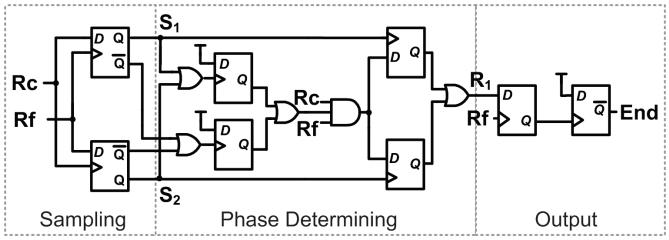

Fig. 7 Proposed phase coincidence detector Circuit

E. Output Counter

The output counter adapted sense-amplified flip-flop (SAFF), as the major circuit to fit high operation frequency and reduced dead zone [6]; by eight serial SAFF-based triggered flip-flop (TFF), the structure of the counter is formed in Fig. 8. To ensure the stability of the counter under high-frequency operating, the output of the second stage is exploited as triggering clock to drive the latter six stages.

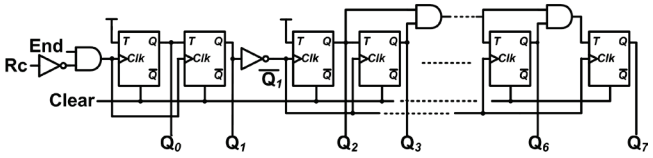

Fig. 8 Proposed counter

Under the condition of the rising edge of *STOP* signal near the rising edge of START signal, CNT_C is unable to cut off immediately due to the lack of time, thus CNT_C erroneously gains one more count. Modifying the disable signal of CNT_C uses the same END signal from the PCD to stop both counters when R_c and R_f signal coincidence can prevent this problem from accruing. The modified timing diagram is shown in Fig. 9, after the arrival of STOP signal, CNTC will additionally record NF cycle, which is the exact cycles as CNTF recorded, and hence the input time is measured as:

$$\begin{aligned} T_{in} &= (N_c + N_f - N_f) \times T_c + (N_f - 2)(T_c - T_f) \\ &= (N_c + N_f - N_f) \times \frac{T_1}{32} + (N_f - 2)(\frac{T_1}{32} - \frac{T_2}{32}) \end{aligned} \tag{5}$$

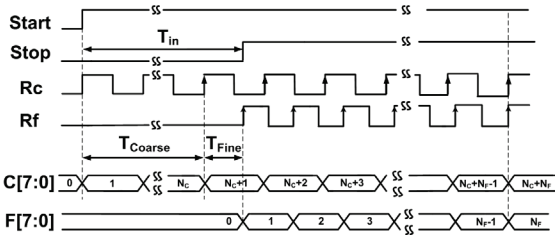

Fig. 9 Time diagram of the proposed TDC

III. Experimental Results

The proposed all digital time-to-digital converter has been fabricated in a 0.18 um CMOS process. The chip microphotograph is shown in Fig 10, which the core area is 309 μm×205 μm. To minimize the noise effect and process variation, some critical points are needed to focus on. By offering three separated power lines to the delay element, remaining digital circuit and the output buffers, the noise affection is greatly minimized. Special care should be taken for the matching of the delay element, so that all the delay elements are placed as close as possible including the use of figure skill and dummy skill. Finally, the signal transmission path, including the bounding wire, should be as matching as compatible to ensure no surplus time delay between *START* and *STOP* signal.

In the measurement, the external reference clock T1 and T2 are given the frequency of 243.902 MHz and 253.807 MHz. Thus with the self-calibrate function, we expect the two delay element have the delay time of 128.125 ps and 123.125 ps. According to Eqs. (2) and (3), the coarse resolution T_C is calculated as 1281.25 ps, and the fine resolution $\triangle$T is measured as 10ps. As mentioned in Eq. (5), we can further derivate the measured time difference. Five measurements for each input interval are collected and plotted as the measured characteristic curve in Fig. 11.

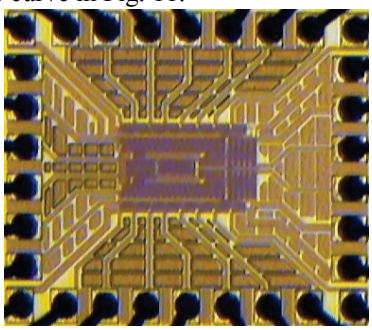

Fig. 10 Microphotograph of the fabricated chip

The specification table with an additional comparison of other TDC technologies is shown in Table I. By using two-stage technique, the input range is greatly increased, while a comparative high resolution of 10 ps is obtained with the use of VDL, and with all digital structure, the power dissipation is greatly reduced under 10 mW.

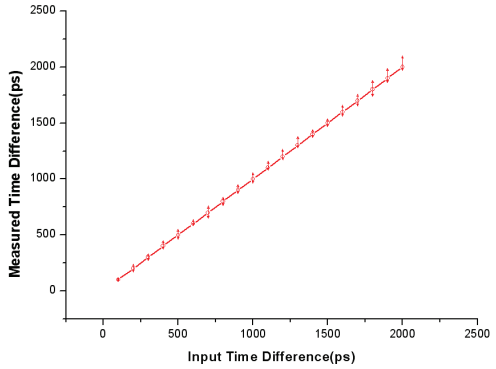

Fig. 11 Input time difference vs. measured time difference

IV. Conclusion

The proposed TDC based on single-stage VDL structure with self-calibrate DLL has utilized at all digital structure and the proposed DCO to achieve high resolution and wide detect range, with the resolution of coarse tune between 0.871~1.388 ns and the fine tune between 10~80.6 ps. A feature of the proposed TDC contains tunable resolutions for easier combination with the system which only has the requirement of two reference clocks. The chips are fabricated in a 0.18-um CMOS process with the core area squared 0.309×0.205 mm^2, and the stable power dissipation of 5.55 mW and dynamic power dissipation of 9.346 mW. The entire digital structure not only retains the advantages of analog designs, but other advantages such as lower power dissipation, smaller core area, the possibility of process scale down and faster conversion time.

TABLE I
SPECIFICATION TABLE

	This Work	[7]	[8]	[9]
Supply Voltage	1.8V	1.8V	1.8V	1.8V
Process (um)	0.18	0.18	0.18	0.18
LSB Width (ps)	10	28	6	61
Input Range(*1)	162ns	7.2ns	-	750ns
Clock Freq. (MHz)	225~317	113~158	100	2~40
Power Dissipation (mW)	5.55(*2) 9.34(*3)	87.7	21	18
Core Area (mm^2)	0.064	1.440	0.042	0.424

(*1) Input range = $Max_{\text{input cycle time range}} - Min_{\text{input pulse width}}$

(*2) Stable power dissipation

(*3) Dynamic power dissipation

Acknowledgment

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