A Folded-Cascode OP Amplifier with a Dynamic Switching Bias Circuit

Hiroo Wakaumi, *Member, IAENG*

***Abstract*—A high-speed folded-cascode OP amplifier with a dynamic switching bias circuit, which enables low power consumption, high gain stably, and a relatively wide dynamic range in low power supply voltages, is proposed. Through simulations, it was shown that the OP amplifier is able to operate at a 10 MHz dynamic switching rate and a dissipated power of 71 % of that observed in continuous operation. It also showed an open loop gain of 51 dB and a 0.996 V output dynamic range which is wider than that in a telescopic OP amplifier. The 10 MHz high-speed switching operation, allowing processing video signals, was confirmed by applying to a switched capacitor non-inverting amplifier with a gain of below 2. The simulation results showed that the output inaccuracy for a switched capacitor amplifier with a gain of below 2 is below 1.5 %, which is practicable. This inaccuracy was caused by the static nonlinearity of the OP amplifier, determined on its limited open loop gain.**

***Index Terms*—switched capacitor circuit, CMOS, operational amplifier, dynamic switching**

I. Introduction

In recent years, the trend of IC development is moving toward lower power consumption using low power supply voltages and short channel CMOS technologies to achieve portable equipment using audio signal processors or video signal processors for use in electrical appliances. Analog signal processors are promising for these applications instead of digital signal processors which have the disadvantage of larger chip area and large power consumption [1,2]. Especially, the CMOS switched capacitor (SC) technology suitable for realizing analog signal processors has promising use in video signal bandwidth circuits in particular, because one can easily integrate complicated systems into a single chip IC at low cost using this technology. It has been demonstrated that SC techniques using CMOS operational amplifiers (OP Amps) are useful for implementing analog functions such as filtering [3,4]. Although CMOS Op Amps are suitable for such filter ICs, the use of several OP Amps results in large power consumption. A high-speed CMOS OP Amp consisting of a fully differential operational transconductance amplifier (OTA) with two pairs of folded-cascade OP Amps and a common-mode-feedback (CMFB) circuit has lately been developed [5]. However, this circuit was too complicated for the signal processing IC, and so required a larger chip area and larger power consumption. Accordingly, a simple OP Amp configuration that enables lower power consumption and smaller chip area, even when the number of OP Amps increases, is desirable for large-scale ICs for multi-functional analog processing.

Until now, several approaches have been considered to decrease the power consumption of OP Amps, including the development of ICs that work at low power supply voltages. A clocked current bias scheme for folded cascade OP Amps has typically been proposed to decrease the power consumption of the OP Amp itself [6,7]. In such a circuit, each bias current for the slewing, settling, and holding phases is dynamically controlled by a multi bias current control method with clocked current sources. Even using this scheme, however, the maximum ratio of the total power savings is limited to near 30 %. Because the circuit also requires complicated four-phase bias-current control pulses and biasing circuits, it results in a large layout area and is not suitable for the high-speed operation.

A control method using power supply switching has been proposed for audio signal processing as another approach in decreasing the power consumption of OP Amps [8]. Because large capacitors for the power supply terminals are intrinsically loaded, the switching speed is limited to a low speed of 1 MHz at most. Therefore, this type of control circuit is not suitable for application to video signal processing ICs, which are required to operate at over 10 MHz switching frequency.

A two-stage OP Amp with resistive biasing consisting of a low-swing folded-cascode amplifier and a high-swing amplifier for high gain and low power consumption has been also proposed [9]. This OP Amp, however, uses a resistor pair (for charging coupling capacitors as a level shifter) connected with a common mode feedback (CMFB) circuit. Therefore, it is not suitable for integration of circuit elements as ICs because of its inaccurate resistor values and instability.

The author previously proposed CMOS OP Amps with a dynamic switching bias circuit, of simple configuration, to provide low power consumption while maintaining high speed switching operation suitable for processing video signals [10,11]. However, the three-stage one of these has a disadvantage which is difficult to operate at low power supply voltages due to the instability. The two-stage one of these has also a demerit that problems of gain restraint and narrow bandwidth operation occur due to the instability in high frequencies when the power supply voltage is reduced. On the contrary, telescopic OP Amps are known to be suitable for implementing high gain [12]. However, it has a problem of a

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H. Wakaumi is with the Division of Electronics and Information Engineering, Tokyo Metropolitan College of Industrial Technology, 1-10-40 Higashi-Ooi, Shinagawa, Tokyo, 140-0011 Japan (corresponding author to provide phone: +81-3-3471-6331; fax: +81-3-3-471-6338; e-mail: wakaumi@s.metro-cit.ac.jp).

narrow dynamic range.

In this paper, a high-speed folded-cascode OP Amp with a dynamic switching bias (DSB) circuit [13], is proposed, which enables low power consumption and is suitable for achieving high gain with wide and stable bandwidths and a relatively wide dynamic range even when power supply voltages are reduced.

II. DSB Folded-Cascode OP Amp

Figure 1 shows a configuration of a folded-cascode OP Amp with a dynamic switching bias circuit (DSBFC OP Amp). The power supply voltages of this circuit are reduced to half (±2.5 V) of those in the conventional DSB OP Amps [10,11] for implementing low power dissipation. The DSB method is also used for implementing lower power dissipation. In the conventional DSB OP Amps, when the power supply voltage is reduced, their gains are restrained and wide bandwidth operation becomes impossible due to the instability. So, in this circuit, a folded-cascade OP Amp circuit is constructed to achieve high gain and wide bandwidth in a stable manner. It is also for achieving a wider dynamic range than that in conventional telescopic OP Amps. In this OP Amp, p-MOS FETs of M10-M13 form current mirror circuits. n-MOS FETs of M8-M9 and M14-M15 form current sources. By replacing a p-channel input differential circuit consisting of a pair of p-MOSFETs in the conventional telescopic OP Amp with a differential input circuit consisting of n-MOSFETs M5-M7, a source voltage of p-MOSFET M13 in a current mirror is raised as compared with that in the conventional telescopic OP Amp. As a result, the dynamic range of the folded-cascode OP Amp is increased. Current sources of M5, M8, and M15 are also turned on/off by controlling a bias voltage of V_B, switching a DSB circuit dynamically to reduce the power consumption still more.

In Fig. 1, the DSB circuit consisting of M1-M4 provides the bias voltage V_B. Figure 2 shows operation waveforms of the DSBFC OP Amp. An external control pulse ϕ_B with a voltage swing of (−2.5 V)−(+2.5 V) drives an inverting switching circuit consisting of the MOSFETs M1-M4. When ϕ_B becomes −2.5 V, the OP Amp turns on by setting a bias voltage V_B at an appropriate level by enabling M3 and M4 to operate in the saturation region, and operates normally as an operational amplifier. Conversely, when ϕ_B becomes +2.5

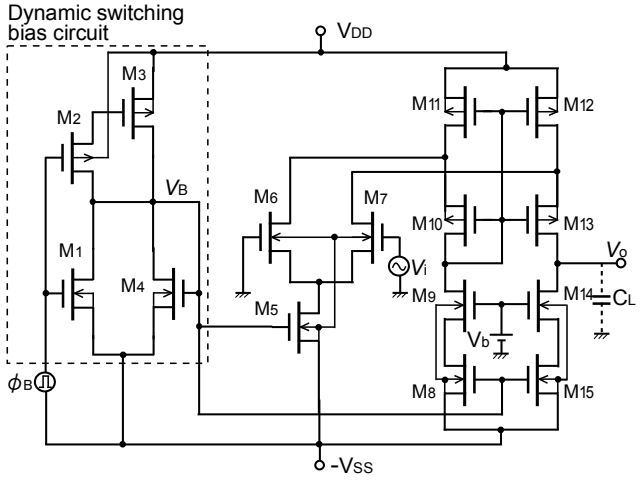

Fig. 1. Configuration of the folded-cascode OP Amp with a DSB circuit.

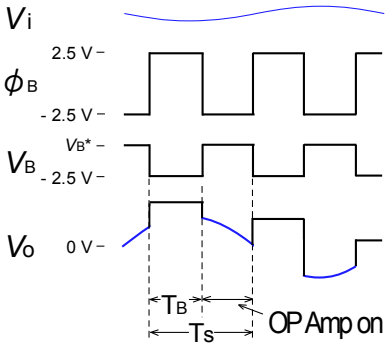

Fig. 2. Operation waveforms of the folded-cascode OP Amp with a DSB circuit.

V, the OP Amp turns off by setting V_B at nearly −2.5 V, enabling M1 to operate in a low impedance and M3 in a high impedance. This high impedance status of M3 occurs because the gate of M3 is set at a potential determined by the capacitance coupling between gate and source of M2 and between gate and drain of M3 at the transition of ϕ_B from −2.5 V to +2.5 V. Therefore, the OP Amp does not dissipate at all during this off period. It is thus expected that the power consumption becomes lower than that observed in usual continuous operation as for the conventional OP Amps.

III. Simulation Results

The DSBFC OP Amp performance was tested through SPICE simulations under the condition of the power supply voltages V_{DD}=V_{SS}=2.5 V. A minimum channel length of p-MOS FETs and n-MOS FETs is 2.5 μm. The channel widths of designed MOSFETs M13, M14, and M7 (deciding mainly the DSBFC OP Amp gain) are 1000 μm, 720 μm, and 1875 μm, respectively, as shown in Table I. The bias voltage V_b of the current source consisting of M9 and M14 is 0.2 V.

Typical performances compared with those of the conventional DSB three-stage OP Amp are shown in Table II. The open loop gain was 358 (51 dB) which is near that of the conventional DSB three-stage OP Amp. The unity gain frequency was 709 MHz. The phase margin was 34.2 degrees. The slew rate of 140 V/μs for a 10 pF load capacitance, which indicates operability for video signals, was obtained from an output response waveform of the unity gain buffer for a 1 $V_{0\text{-}P}$ input pulse signal. However, its high peak voltage of 0.977 V was a little smaller than 1.0 V. This indicates that the output dynamic range is not enough wide. Figure 3 shows static input-output characteristics of the DSBFC OP Amp. When a 10 % distortion is allowable, the output dynamic range was 0.996 V, which is wider than that (0.74 V) in a telescopic OP Amp with a nearly equal gain. When a 1 % distortion is also permitted, the output dynamic range for the DSBFC OP Amp

Table I. Designed channel length L and width W of the FETs.

FET	W/L (μm/μm)	FET	W/L (μm/μm)
M1	7.5/2.5	M6, M7	1875/2.5
M2	15/2.5	M8, M15	62/2.5
M3	10/4	M9, M14	720/2.5
M4	53/6	M10, M13	1000/2.5
M5	105/2.5	M11, M12	90/2.5

Table II. Typical performances for the new DSB folded-cascode and conventional three-stage DSB OP Amps.

	DSB folded-cascode OP Amp	DSB three-stage OP Amp
Power supply voltage [V]	±2.5	±5
Minimum channel length [μm]	2.5	2.5
Switching frequency [MHz]	10	10
Open gain [dB]	51	53.8
Slew rate [V/μs]	140	336
Settling time [ns]	12	24
Power dissipation [mW] (in continuous operation)	24	143
Power dissipation [mW] (in 50 % switching duty ratio)	17	86

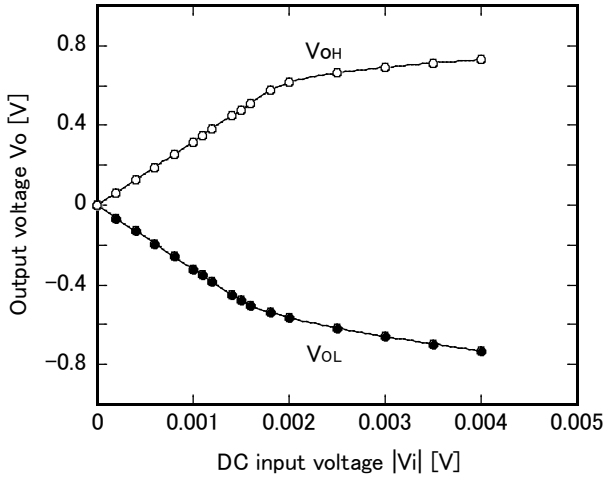

Fig. 3. Static input-output characteristics.

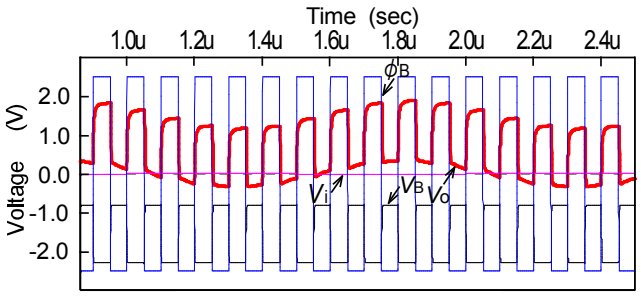

Fig. 4. Simulation waveforms of the folded-cascode OP Amp with a DSB circuit. Input signal frequency f_{in}=1 MHz, V_{in}=0.001 $V_{0\text{-}P}$, f_S=10 MHz, C_L=1.0 pF.

was 0.6 V, which is larger than that (nearly 0.5 V) in the telescopic OP Amp. These show that this OP Amp possesses the relatively wide output dynamic range, high gain, and stability in a wide bandwidth.

The DSBFC OP Amp operated in a dynamic switching mode with a duty ratio of 50 % and a switching frequency, fs, of 10 MHz as shown in Fig. 4. Because the output sine wave voltage was nearly equal to that in the static mode of the DSBFC OP Amp, there seems to be hardly any distortion caused by making the DSBFC OP Amp to do dynamic switching operation. In the operation mode of 50 % duty ratio, the power dissipation was 17 mW, which is 71 % of that observed in the static operation mode (Fig. 5). This is also nearly 1/5 of that (86 mW) in the conventional three-stage OP Amp, which shows this OP amp's low power characteristics

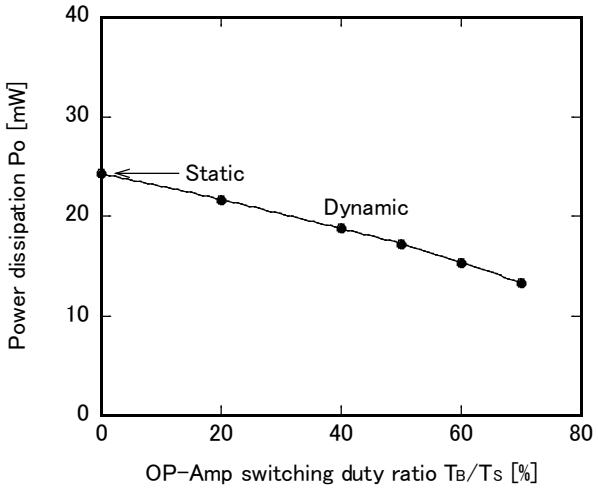

Fig. 5. Power dissipation vs. OP-Amp switching duty ratio in the DSB mode. f_S=10 MHz.

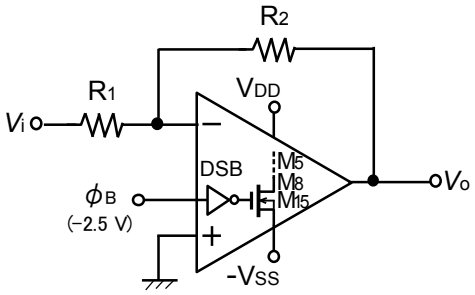

Fig. 6. Configuration of the inverting amplifier with the DSB folded-cascode OP Amp. R_1=500 kΩ, R_2=1 MΩ.

due to the reduced effect of power supply voltages (half of that in the conventional three-stage OP Amp) and dynamic switching operation.

To evaluate the inherent static nonlinearity of the DSBFC OP Amp, the total harmonic distortion (THD) was tested. The THD for the 0.835 $mV_{0\text{-}P}$ input signal (10 kHz), enabling 0.6$V_{p\text{-}p}$ to output, was only 0.4 %. This is extremely small. Considering the real application of the DSBFC OP Amp, the nonlinearity for a circuit configuration of the inverting amplifier with the negative feedback circuit element needs to be evaluated. So, the output voltage inaccuracy of the inverting amplifier (Fig. 6) consisting of resistors R_1 (=500 kΩ) and R_2 (=1 MΩ) and the present OP Amp was tested. Figure 7 shows the output voltage inaccuracy versus the DC input voltage for the inverting amplifier at a gain of 2. The inaccuracy ε' defined by $2|V_i|-|V_o|$ for the input voltages between 0.3 and −0.3 V was less than 6 mV, which is below 1.0 % of the theoretical output voltage ($2|V_i|$). This inaccuracy is near a theoretical value of 0.83 %, determined mainly by the open loop gain of the OP Amp.

IV. Application to SC Amplifier

To demonstrate the practicability of the above DSBFC OP Amp, the feasibility of its application in an SC non-inverting amplifier which can be used for processing circuits such as filters, was tested. Figures 8 and 9 show the SC non-inverting amplifier configuration and operation waveforms, respectively. Switches in the SC amplifier are driven by complementary operating pulses φ_1 and φ_2. These switches consist of CMOS

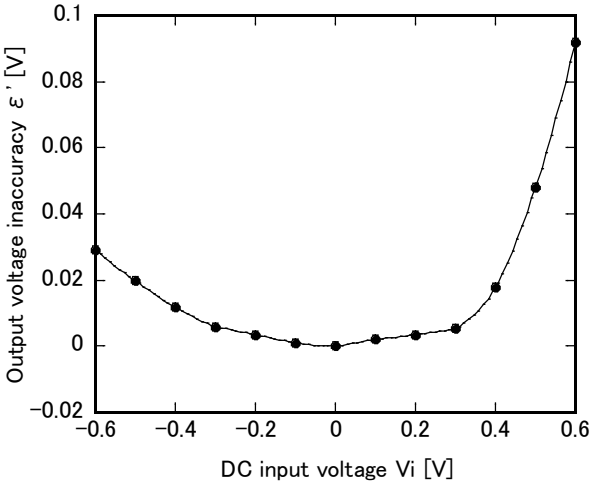

Fig. 7. Output voltage inaccuracy vs. DC input voltage for the inverting amplifier using the DSB folded-cascode OP Amp. The gain R_2/R_1 is 2.

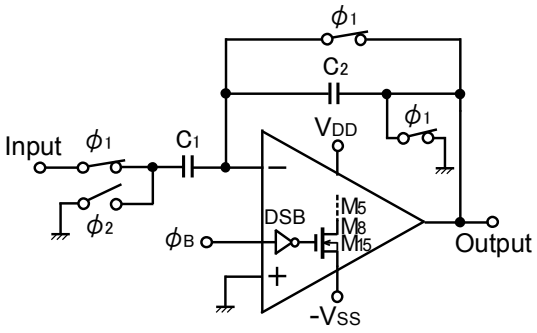

Fig. 8. Configuration of the SC non-inverting amplifier. φ_1 and φ_2 switches consist of CMOS FETs with W/L=25/2.5 (μm/μm).

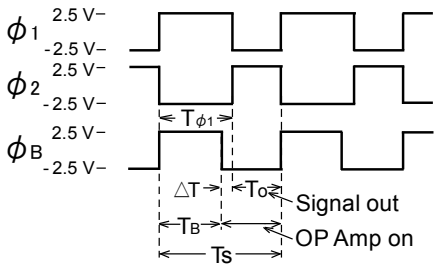

Fig. 9. Operation waveforms of the SC non-inverting amplifier.

FETs with a channel width / channel length W/L=25/2.5 (μm/μm). When the sampling pulse φ_2 changes from a low level (−2.5 V) to a high level (2.5 V), the amplified sampled input signal is output during the on-state of the OP Amp (φ_B is low). φ_B is set to low just before φ_2 changes to high (10 ns was chosen for the transition delay time against the φ_B fall transition as in the previous three-stage OP Amp circuit) such that the sampled input signal is amplified in the DSBFC OP Amp in a stable manner. Operation waveforms with a gain (C_1/C_2) of 2 show that this OP Amp can operate within a bandwidth of over 2 MHz at fs=10 MHz as shown in Fig. 10. When the switching duty ratio T_B/Ts of the OP Amp was 50 %, the power dissipation of the SC amplifier was nearly 70 % of that observed during static operation (Fig. 11). It is just 5.7 mW larger than that of the DSBFC OP Amp. This additional

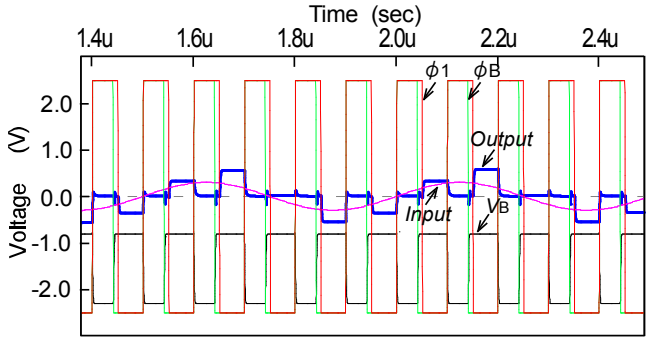

Fig. 10. Simulation waveforms for the SC non-inverting amplifier. C_1=1.2 pF, C_2=0.6 pF, ΔT=10 ns. Output load C_O=1.0 pF. Input signal=0.3 $V_{0\text{-}P}$, Input signal frequency f_{in}=2 MHz.

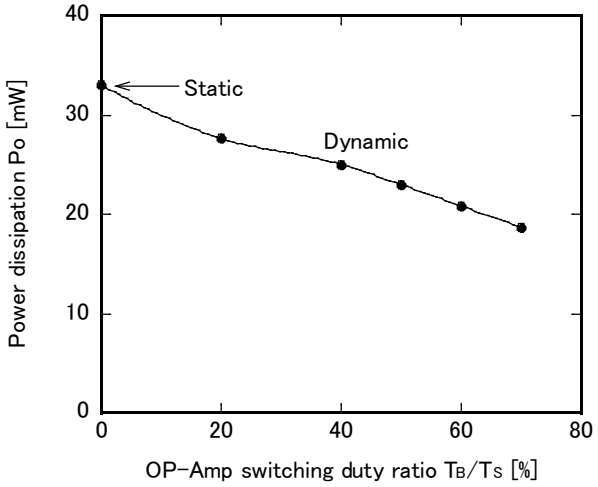

Fig.11. Power dissipation vs. OpAmp switching duty ratio in the SC amplifier. C_1/C_2=2. fs=10 MHz, ΔT=10 ns. Input signal=0.3 $V_{0\text{-}P}$, fin=2 MHz.

power dissipation was dissipated in the switches. By increasing the duty ratio T_B/Ts to 70 %, its power dissipation decreased to 57 % of that observed during the static operation.

This DSBFC OP Amp with such high speed and low power consumption characteristics can be modified to a carbon nanotube (CNT) based OP Amp by replacing sink FETs (M1, M4-M9, M14, M15) with carbon nanotube field effect transistors (CNTFETs), such as a CNT based operational transconductance amplifier [14]. Because these CNTFETs have high mobility [15,16], the achievement of higher speed operation is expected. Therefore, a higher speed SC amplifier should be realized by using the CNT based OP Amp.

The accuracy of the output voltage was tested using parameters important in practical applications. Figure 12 shows the output voltage inaccuracy versus the OP Amp switching duty ratio in the SC amplifier at a gain of 2. Here, the output voltage inaccuracy ε represents the difference between a theoretical value of the output voltage (gain × input voltage) and the actual output voltage. When the switching duty ratio T_B/Ts was 0−60 %, the inaccuracy ε for the 0.6 $V_{p\text{-}p}$ input signal was below 1.5 % of the theoretical output voltages, which is practicably usable. It is thought that this inaccuracy was mainly caused by the nonlinearity in the static operation of the DSBFC OP Amp, determined on its limited open loop gain, because the inaccuracy ε' of the inverting amplifier using the OP Amp was nearly 1.0 %.

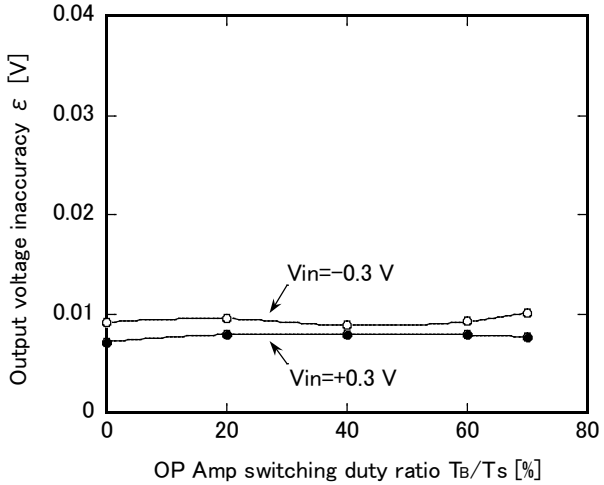

Fig. 12. Output voltage inaccuracy vs. OP-Amp switching duty ratio in the SC non-inverting amplifier. C_1/C_2=2. fs=10 MHz, ΔT=10 ns.

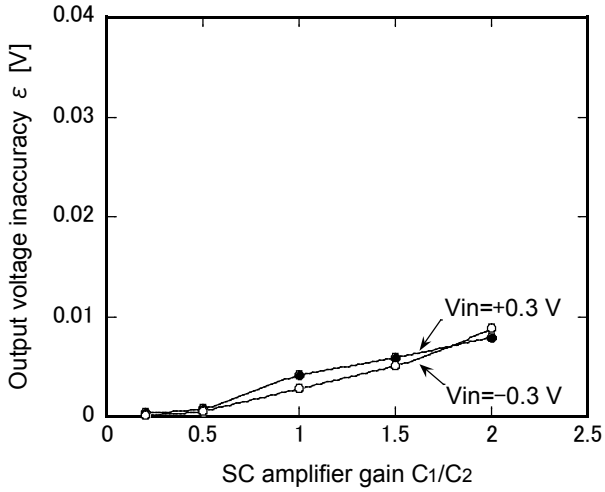

Fig. 13. Output voltage inaccuracy vs. SC amplifier gain. $T_{\varphi 1}$=50 ns, ΔT=10 ns.

The gain dependency of the inaccuracy was tested, considering several OP Amps used in the form of different gains in the filters. Figure 13 shows the output voltage versus the SC amplifier gain. The inaccuracy ε increased almost linearly with gain and was below 1.5 % of theoretical output voltages within the gain of 2.

V. Conclusions

A high-speed folded-cascode OP Amp with a dynamic switching bias circuit capable of processing video signals, which enables low power consumption, high gain with wide and stable bandwidths, and a wide dynamic range in low power supply voltages, was proposed. Through simulations, it was shown that the OP Amp is able to operate at a 10 MHz dynamic switching rate and a dissipated power of 71 % of that observed in continuous operation. It also showed an open loop gain of 51 dB and a 0.996 V output dynamic range which is wider than that in a telescopic OP Amp. The 10 MHz high speed switching operation, allowing processing video signals, was confirmed by application to a switched capacitor non-inverting amplifier with a gain of below 2. The simulation results showed that the output inaccuracy for a switched capacitor amplifier within a gain of 2 was below 1.5 %, and was mainly caused by the static nonlinearity of the OP Amp, determined on its limited open loop gain.

This circuit should be useful for the realization of low-power wide-band signal processing ICs. It might be also modified as the CNT based OP Amp, which is expected to be employed for high speed drive use.

References

[1] S. Nakagawa, H. Terane, T. Matsumura, H. Segawa, M. Yoshimoto, H. Shinohara, S. Kato, M. Hatanaka, H. Ohira, Y. Kato, M. Iwatsuki, K. Tabuchi, and Y. Horiba, "A 24-b 50-ns Digital Image Signal Processor," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 6, pp. 1482-1493, Dec. 1990.

[2] T. Minami, R. Kasai, H. Yamauchi, Y. Tashiro, J. Takahashi, and S. Date, "A 300-MOPS Video Signal Processor with a Parallel Architecture," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 12, pp. 1868-1875, Dec. 1991.

[3] R. Dessoulavy, A. Knob, F. Krummenacher, and E. A. Vittoz, "A Synchronous Switched Capacitor Filter," *IEEE Journal of Solid-State Circuits*, vol. SC-15, no. 3, pp. 301-305, June 1980.

[4] J.-T. Wu, Y.-H. Chang, and K.-L. Chang, "1.2 V CMOS switched-capacitor circuits," in *1996 IEEE International Solid-State Circuits Conf. Digest of Technical Papers-42nd ISSCC*, pp. 388-389, 479.

[5] A. Ahmadpour and R. Fouladi, "A Modified High-Performance Structure of Low-Voltage CMOS Op-amp,"in *IEEE International Conf. on Electron Devices and Solid-State Circuits 2008-EDSSC 2008*, pp. 1-5.

[6] D. B. Kasha, W. L. Lee, and A. Thomsen, "A 16-mW, 120-dB Linear Switched-Capacitor Delta-Sigma Modulator with Dynamic Biasing," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, pp. 921-926, July 1999.

[7] H. L. Chen, Y. S. Lee, and J. S. Chiang, "Low Power Sigma Delta Modulator with Dynamic Biasing for Audio Applications," in *50th Midwest Symposium on Circuits and Systems 2007-MWSCAS 2007*, pp. 159-162.

[8] H. Wang, J. Xu, and X. Wu, "A low Power Audio Delta-Sigma Modulator with Opamp-Shared and Opamp-Switched Techniques," in *Proc. of the International Multiconference of Engineers and Computer Scientists 2010-IMECS 2010*, vol. Ⅱ, pp. 1296-1300.

[9] S. H. Mirhosseini and A. Ayatollahi, "A Low-Voltage, Low-Power, Two-Stage Amplifier for Switched-Capacitor Applications in 90 nm CMOS Process," *Iranian Journal of Electrical & Electronic Engineering*, vol. 6, No. 4, pp. 199-204, Dec. 2010.

[10] H. Wakaumi, "A High-Speed CMOS OP Amplifier with a Dynamic Switching Bias Circuit," *SICE Journal of Control, Measurement, and System Integration*, vol. 6, no. 6, pp. 376-380, Nov. 2013.

[11] H. Wakaumi, "A High-Speed Three-Stage CMOS OP Amplifier with a Dynamic Switching Bias Circuit," *Engineering Letters*, vol. 21, issue 4, pp. 218-223, Dec. 2013.

[12] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, Hoboken: John Wiley & Sons, 3rd ed. 2010, pp. 733-735.

[13] H. Wakaumi, "A Folded-Cascode OP Amp with a Dynamic Switching Bias Circuit," in *Proc. of 2014 IEEE Asia Pacific Conf. on Circuits and Systems-APCCAS2014*, pp. 53-56.

[14] S. A. Loan, M. Nizamuddin, F. Bashir, H. Shabir, A. M. Murshid, A. R. Alamoud, and S. A. Abbasi, "Design of a Novel High Gain Carbon Nanotube based Operational Transconductance Amplifier," in *Proc. of the International MultiConference of Engineers and Computer Scientists 2014-IMECS 2014*, vol. Ⅱ, ISBN: 978-988-19253-3-6.

[15] F. A. Usmani and M. Hasan, "Carbon nanotube field effect transistors for high performance analog applications: An optimum design approach," *Microelectronics Journal*, vol. 41, pp. 395-402, May

2010.

[16] Y.-B. Kim, "Integrated Circuit Design Based on Carbon Nanotube Field Effect Transistor," *Trans. Electrical and Electronic Materials*, vol. 12, no. 5, pp. 175-188, Oct. 2011.

Hiroo Wakaumi became a Member of IAENG in 2013. He received his B.E. in Electronics from Chiba University in 1973 and his Ph.D. in Electrical Engineering from Tokyo Metropolitan University in 2000.

Until 1992, he worked at NEC Corporation. He then joined Tokyo Metropolitan College of Technology, now Tokyo Metropolitan College of Industrial Technology, in 2006, where he is currently a professor. His research interests include CCDs, display devices, high-voltage MOS ICs, magnetic sensing, optical sensing, and signal processing.

Prof. Dr. Wakaumi has published four books and more than 130 publications including journals and international conference papers. He is a senior member of both the IEEE and IEICE, and is also a member of SICE and an editorial member of AASCIT. He was awarded a best invited paper award at the international conference of CIM'07.