Grounded FDNC and FDNR Realizations Based on G_m-C Technique and Their Applications to Ladder Filter Design

Sasitaporn Theingjit, Tattaya Pukkalanun, and Worapong Tangsrirat, *Member, IAENG*

***Abstract*— A simple circuit for the realization of the grounded frequency-dependent negative conductance (FDNC) using active transconductance (G_m) elements is discussed. Based on the realized FDNC as a fundamental circuit element, the frequency-dependent negative resistances (FDNR) can also be obtained. The equivalent values of the realized elements can be adjusted electronically by means of the transconductance parameters. Both simulator circuits do not require the component-matching condition, and enjoy employing only G_m-cells together with two grounded capacitors; accordingly, they are canonical structures and convenient for integration. Simulation results with TSMC 0.35-μm CMOS technology are presented to validate the characteristics of the realized simulator circuits and their applications.**

***Index Terms*— Transconductance cell (G_m-cell), Frequency-Dependent Negative Conductance (FDNC), Frequency-Dependent Negative Resistance (FDNR), immittance function**

I. Introduction

FREQUENCY-DEPENDENT NEGATIVE CONDUCTANCE (FDNC) and frequency-dependent negative resistances (FDNR) are useful active elements in the synthesis and design active ladder filters [1]. They can also be used in the realization of chaotic oscillator circuits [2]. Several realizations of FDNC and FDNR simulators using various types of active building blocks were proposed in the literature [3]-[8]. The circuit of [4] uses three current conveyors, and requires component matching condition. The FDNR simulators in [5]-[6] require at least four passive components. Moreover, they also require matching component. In [7]-[8], floating resistors and capacitors were employed that are not preferable for integrated circuit (IC) implementation point of view.

In literature, it is widely accepted that the transconductances cell or G_m-cells are fundamental circuit elements for the realization of many analog active circuits and systems, especially in the design of modern electronic circuit building blocks, such as CDTA (current differencing transconductance amplifier), CFTA (current follower transconductance amplifier), VDTA (voltage differencing transconductance amplifier), and CCTA (current conveyor transconductance amplifier) [9]. They are also used in interface circuits, instrumentation amplifiers, and continuous-time-filters [10]. Since the transconductance gain is electronically variable, they can also be applied in automatic, gain control circuits, and analog multipliers.

Considering these facts, the realizations of grounded FDNC and FDNR based on the use of only G_m-cells as basic circuit elements has been described in this study. The circuits are realizable by using only G_m cells and grounded capacitors, without needing passive resistors. It has been shown that the values of the *M*-element and the *D*-element of the realized simulators are controllable electronically through the external biasing currents. In addition, the simulators have been tested in an active realization of the classical *LC* highpass and lowpass ladder filters. To demonstrate the practical workability of the proposed circuits and its applications, simulation results based on TSMC 0.35-μm CMOS process parameters have been provided.

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Sasitaporn Theingjit, Tattaya Pukkalanun, and Worapong Tangsrirat are with the Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Chalongkrung road, Ladkrabang, Bangkok 10520, Thailand (phone: 662-326-4205; fax: 662-326-4205; e-mail: worapong.ta@kmitl.ac.th).

II. CMOS Realization of Basic G_M-Cell

A particularly simple CMOS realization and the symbol of the tunable G_m cell, which will be used as a fundamental circuit for implementing the proposed circuit, are shown in Fig.1(a) and 1(b), respectively. The circuit is mainly composed of two Arbel-Goldminz transconductances [11]. For this element, the transconductance value can be determined by the output transistor transconductance, which can be approximated as:

$$G_m \cong \left(\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}}\right)+\left(\frac{g_{m3}g_{m4}}{g_{m3}+g_{m4}}\right) \qquad (1)$$

where $g_{mi} = [K_{n(p)}I_B]^{1/2}$ (i = 1, 2, 3, 4) and $K_{n(p)}$ is the transconductance parameter of NMOS (PMOS) transistor and I_B is an external DC bias current of this element, respectively. Note that in eq.(1), the value of G_m is electronically tunable by changing the bias current I_B.

III. FDNC Implementation

Fig.2 shows the circuit realization of an electronically tunable grounded FDNC based on three G_m-cells of Fig.1 and two grounded capacitors. This realization is based on the structure given in [12]. It should be noted from Fig.1

that the configuration uses only 12 MOS transistors and all-grounded capacitors, which results in a resistorless and canonical structure. An analysis of the circuit shown in Fig.2 yields the following input impedance as :

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{s^2 C_A C_B}{G_{m1} G_{m2} G_{m3}} = s^2 M \tag{2}$$

where the M-element value is given by :

$$M = \frac{C_A C_B}{G_{m1} G_{m2} G_{m3}} \tag{3}$$

From above relation, it is evident that the FDNC is realized, which is electronically controllable by adjusting G_{m1}, G_{m2} and G_{m3} properly. The circuit comprises only G_m-cell and grounded capacitors; hence, it is suitable for IC fabrication. Moreover, no component matching constraint is required in this realization.

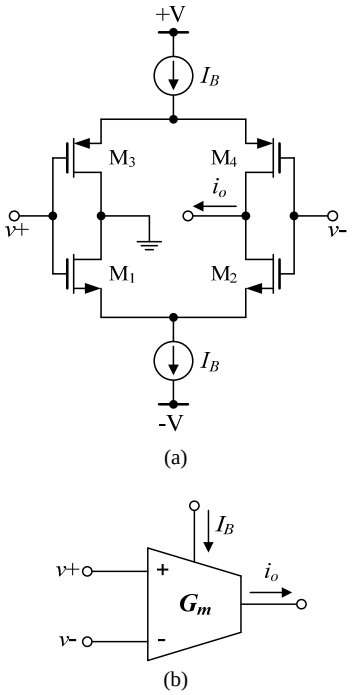

Fig. 1. Basic G_m cell.
(a) CMOS circuit implementation (b) circuit symbol.

Using the classical relation of the circuit sensitivity, i.e.

$$S_x^y = \frac{x}{y}\frac{\partial y}{\partial x} \tag{4}$$

where y denotes the sensitivity parameter which is in this case the M-element value, and x may represent any parameter of the circuit with respect to which the sensitivity is to be evaluated. According to (3)-(4), the active and passive sensitivities of the FDNC in Fig.2 can be obtained as:

$$S_{G_{m1}}^M = S_{G_{m2}}^M = S_{G_{m3}}^M = -1 \tag{5}$$

and

$$S_{C_A}^M = S_{C_B}^M = 1 \tag{6}$$

All sensitivity figures are not higher than unity in magnitude. Therefore, the FDNC of Fig.2 exhibits low active and passive sensitivities.

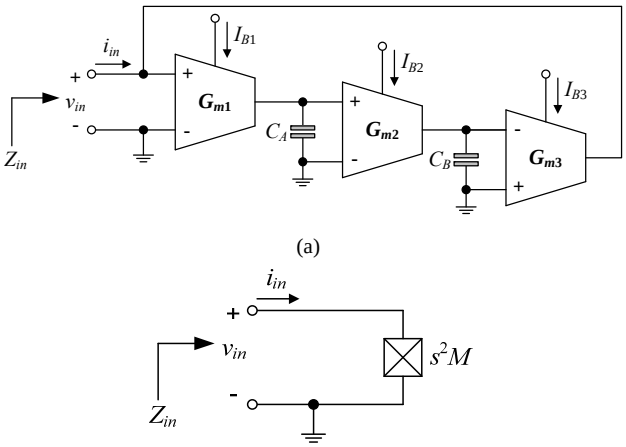

Fig. 2. Grounded FDNC realization with G_m-cells.
(a) G_m-C implementation (b) its circuit symbol.

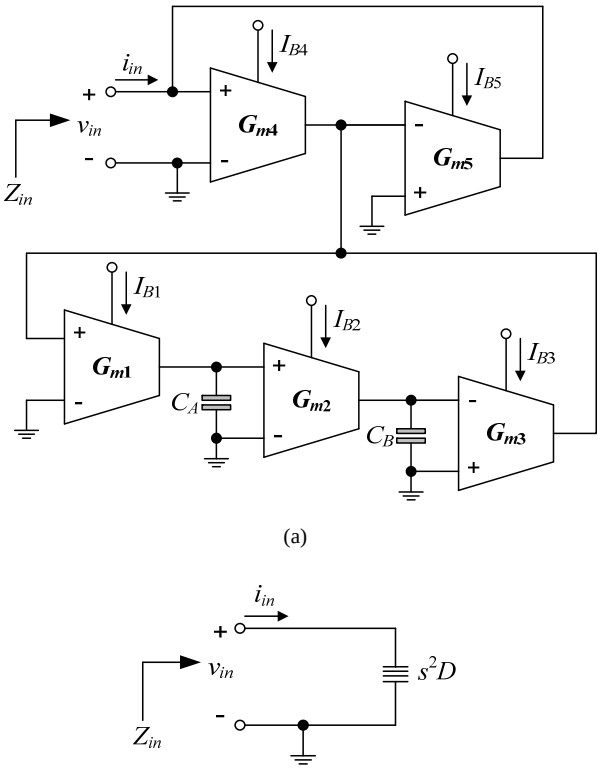

Fig. 3. Grounded FDNR realization based on FDNC of Fig.2.
(a) G_m-C implementation (b) its circuit symbol.

IV. FDNR Implementation

In this section, the generalized circuit topology suitable for grounded FDNR realization is introduced. The introduced FDNR topology is depicted in Fig.3. It is based on the FDNC realization shown in Fig.2, where the G_{m4} and G_{m5} behave the variable impedance converter. The circuit

has the advantage of using all-grounded capacitors, which enables easy implementation in IC form. The input impedance of the circuit is expressed by :

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{G_{m1}G_{m2}G_{m3}}{s^2 C_A C_B G_{m4} G_{m5}} = \frac{1}{s^2 D} \tag{7}$$

Thus, the circuit of Fig.3 simulates a grounded FDNR whose its value is obtained as :

$$D = \frac{C_A C_B G_{m4} G_{m5}}{G_{m1} G_{m2} G_{m3}} \tag{8}$$

Similarly, employing (4), the active and passive sensitivities of the FDNR with respect to the active and passive circuit components are found as :

$$S_{G_{m1}}^{D} = S_{G_{m2}}^{D} = S_{G_{m3}}^{D} = -S_{G_{m4}}^{D} = -S_{G_{m5}}^{D} = -1 \tag{9}$$

and

$$S_{C_A}^{D} = S_{C_B}^{D} = 1 \tag{10}$$

which are within unity in magnitude.

V. Simulation Results and Performance Discussions

To evaluate the behavior of the FDNC and FDNR circuit realizations in Figs.2 and 3, PSPICE simulation has been performed using TSMC 0.35-μm CMOS process model parameters. In simulations, the dimensions W(μm)/L(μm) of the MOS transistors are set to be 16.1/0.7 for M_1-M_2, and 28/0.7 for M_3-M_4. The supply voltages used for the proposed simulator circuit are +V = -V = 1.5 V. According to Fig.1, the bias currents (I_Bs) used in simulations are realized by the simple current mirrors.

The impedance-frequency characteristics of the proposed FDNC circuit of Fig.2 for various bias currents are shown in Fig.4. The results were obtained by setting the following passive and active components : $C_A = C_B = 1$ nF and $I_B = I_{B1} = I_{B2} = I_{B3}$ ($G_m = G_{m1} = G_{m2} = G_{m3}$). By tuning I_B = 40 μA, 100 μA, and 200 μA (G_m = 0.38 mA/V, 0.60 mA/V and 0.81 mA/V), thus the FDNC with M = 18.2 nF/s, 4.7 nF/s and 1.9 nF/s are obtained respectively. It confirms from the curves that the impedance values can be adjusted precisely by changing the biasing current I_B. Also, from Fig.4, the circuit works correctly along the range 20 kHz to 300 kHz, approximately.

In order to demonstrate the performance of the FDNR in Fig.3, it was designed with $C_A = C_B = 1$ nF, $I_{BA} = I_{B1} = I_{B2} = I_{B3}$ ($G_{mA} = G_{m1} = G_{m2} = G_{m3}$), and $I_{BB} = I_{B4} = I_{B5}$ ($G_{mB} = G_{m4} = G_{m5}$). In simulations, the circuit was simulated by keeping I_{BB} = 200 μA and varying I_{BA} = 40 μA, 100 μA, and 200 μA, resulting in D = 8.34 fF/s, 3.05 fF/s, and 1.24 fF/s, respectively. Fig.5 shows the theory and simulated frequency characteristics of the FDNR simulator of Fig.3 for various I_{BA} values. As demonstrated in both figures, the realized FDNR works perfectly between 20 kHz and 300 kHz. Also note that the simulation results agree quite well with the prediction values, and confirm that the D–element value can be adjusted electronically by the G_m biasing currents.

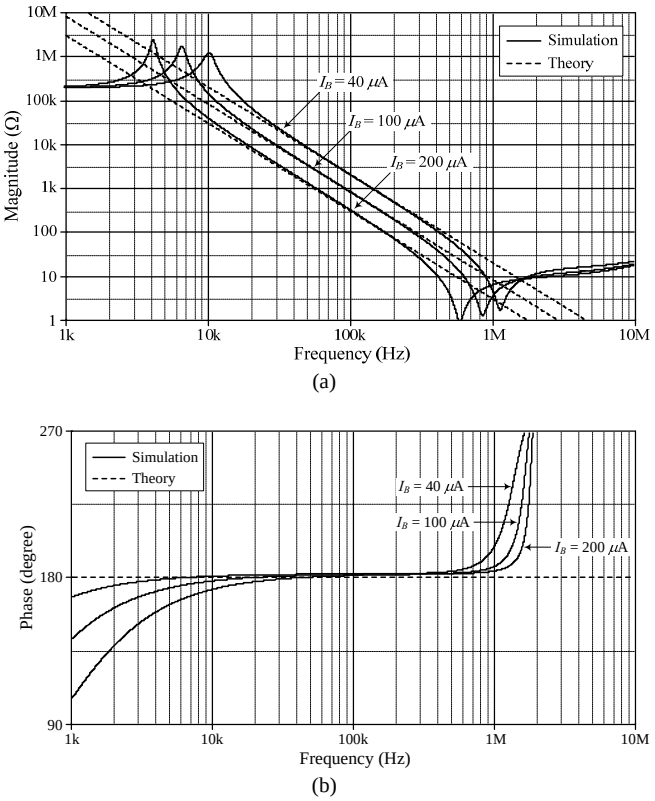

Fig. 4. Theory and simulated frequency characteristics for the grounded FDNC circuit of Fig.2.
(a) magnitude responses (b) phase responses.

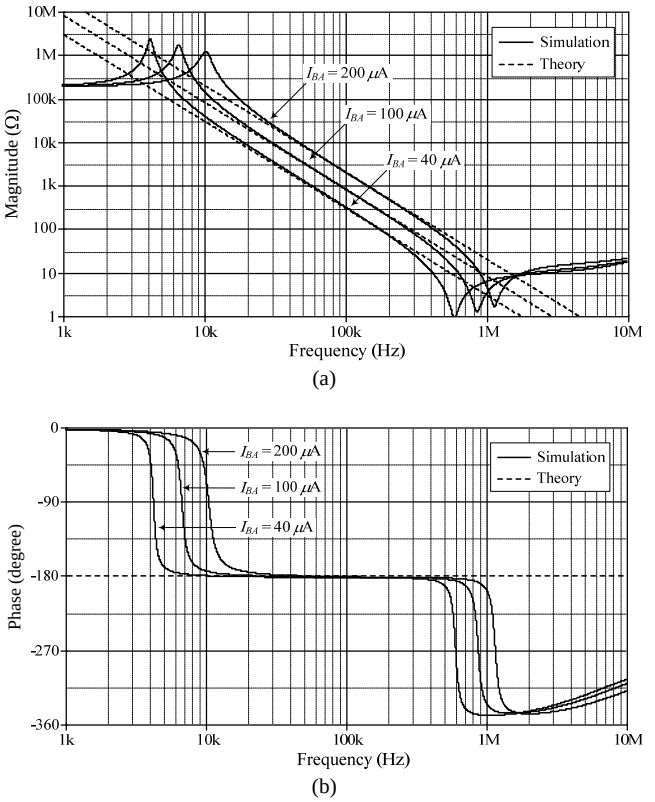

Fig. 5. Theory and simulated frequency characteristics for the grounded FDNR circuit of Fig.3.
(a) magnitude responses (b) phase responses.

VI. Applications to *LC* Ladder Filter Design

A. LC Highpass filter

To evaluate the performance of the FDNC realization of Fig.2 and to demonstrate its application, the third-order *LC* highpass ladder filter shown in Fig.6(a) is used as a prototype network. The normalized design for $\omega_c = 2\pi f_c = 1$ rad/sec was obtained with the following passive component values : $R_s = R_L = 1\ \Omega$, $C_1 = C_3 = 1$ F, and $L_2 = 0.5$ H [13]. To obtain a cutoff frequency of $f_c = 1$ MHz, the variable impedance scaling method has been performed with magnitude scaling constant of $k_m = 300$ and frequency scaling constant of $k_f = 6.28\times10^6$. As a result, the passive component values in Fig.6(a) have been found to be : $R_s = R_L = 300\ \Omega$, $C_1 = C_3 = 530$ pF, and $L_2 = 24\ \mu$H. It is known [12], [14] that it is indeed possible to convert *RLC* passive filter into *RLM*-immittance network by a combination of resistances, inductances and FDNCs. Thus, by employing a network transformation technique for active-*RC* realization of *RLM*-immittances [14], the derived equivalent *RLM* network is obtained as shown in Fig.6(b), where the M_2-element has been designed by using FDNC in Fig.2 with $C_A = C_B = 0.1$ nF, $I_B = I_{B1} = I_{B2} = I_{B3} = 100\ \mu$A ($G_m = G_{m1} = G_{m2} = G_{m3} = 0.60$ mA/V). Using scaling factors $k_m = 3\times10^3$ and $k_f = 6.28\times10^6$, the component values of the transformed *RLM* network in Fig.6(b) are obtained as : $L_{RS} = L_{RL} = 478\ \mu$H, $R_{L1} = R_{L3} = 3$ kΩ, and $M_2 = 46$ pF/s. The simulated magnitude and phase frequency characteristics of both filters in Fig.6 are shown in Fig.7. It can be seen that the responses exhibited from the derived *RLM* network and the *RLC* passive prototype are in good agreement.

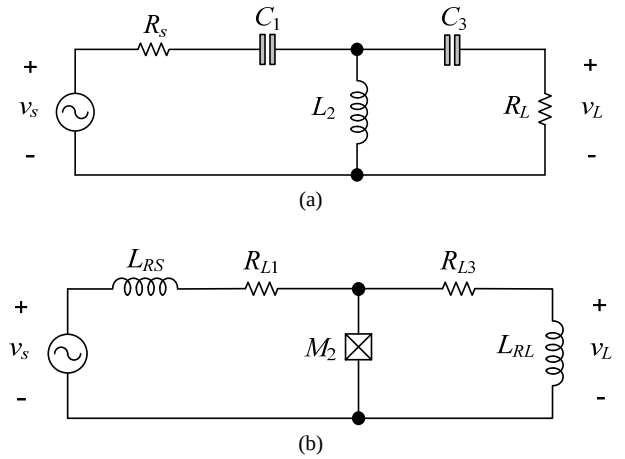

Fig. 6. Third-order highpass *LC* filter.
(a) *RLC* passive prototype (b) equivalent *RLM* network with FDNC of Fig.2.

In addition to the simulations, in order to demonstrate the electronic tunability of the derived *RLM* network in Fig.6(b), the following component values were taken as : $C_A = C_B = 0.1$ nF, and three different values of I_B being 40 μA, 100 μA and 200 μA, which results in $M_2 = 182$ pF/s, 46 pF/s and 19 pF/s, respectively. The three simulated gain responses of the *RLM* network in Fig.6(b) with M_2-tuning are shown in Fig.8, which accordingly demonstrate the current variability of the transformed circuit.

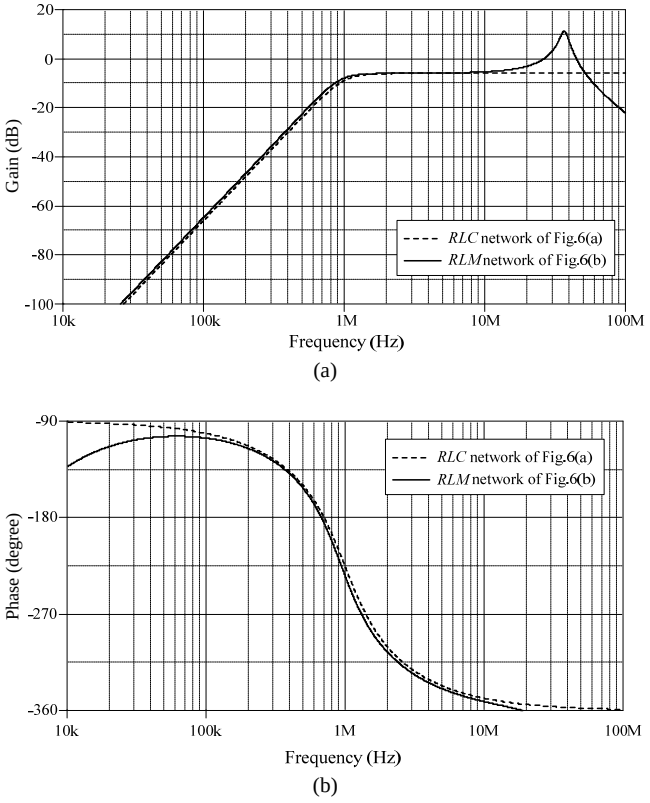

Fig. 7. Simulated frequency responses of the filters in Fig.6.
(a) gain responses (b) phase responses.

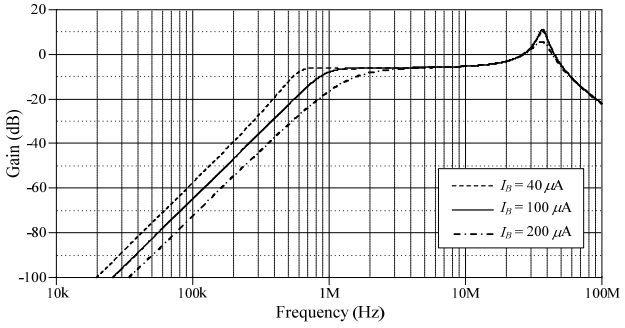

Fig. 8. Simulated gain responses of Fig.6(b) with tuning the M_2-element value.

B. Butterworth lowpass filter

To further illustrate an application of the FDNR realization in Fig.3, the third-order Butterworth lowpass filter was designed and simulated. The normalized *RLC* passive prototype is shown in Fig.9(a), where $R_s = R_L = 3.18$ kΩ, $L_1 = L_3 = 5$ mH, and $C_2 = 1$ nF [13]. The voltage transfer function of the circuit in Fig.9(a) is given by :

$$\frac{V_L(s)}{V_S(s)} = \frac{1}{s^3\left(\frac{L_1L_3C_2}{R_L}\right) + s^2\left(\frac{R_SL_3C_2}{R_L} + L_1C_2\right) + s\left(R_SC_2 + \frac{L_1+L_3}{R_L}\right) + \frac{R_S}{R_L} + 1} \tag{11}$$

By applying Bruton transformation [1] and using appropriate impedance scaling with $k_m = 1.59\times10^3$ and $k_f = 628\times10^3$, the *RLC* passive filter of Fig.9(a) then will have $f_c = 100$ kHz. As a results, the filter is converted into *RCD* network as shown in Fig.9(b), where the FDNR is realized using the configuration of Fig.3. In Fig.9(b), the resulting

circuit components are obtained as : $C_{RS} = C_{RL} = 1$ nF, $R_{L1} = R_{L3} = 1.59$ kΩ, and $D_2 = 3.18$ fFs. The results of PSPICE simulation of an illustrative example filter are also given, verifying the proper operation. Fig.10 shows the magnitude and phase characteristics of the filters in Fig.9. It is seen from the results of Fig.10 that simulation results corresponds well with the expectation ones.

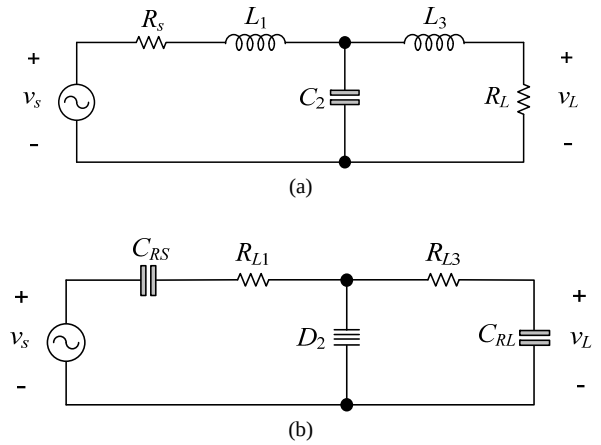

Fig. 9. Third-order Butterworth lowpass filter.
(a) RLC passive prototype (b) equivalent *RCD* network with FDNR of Fig.3.

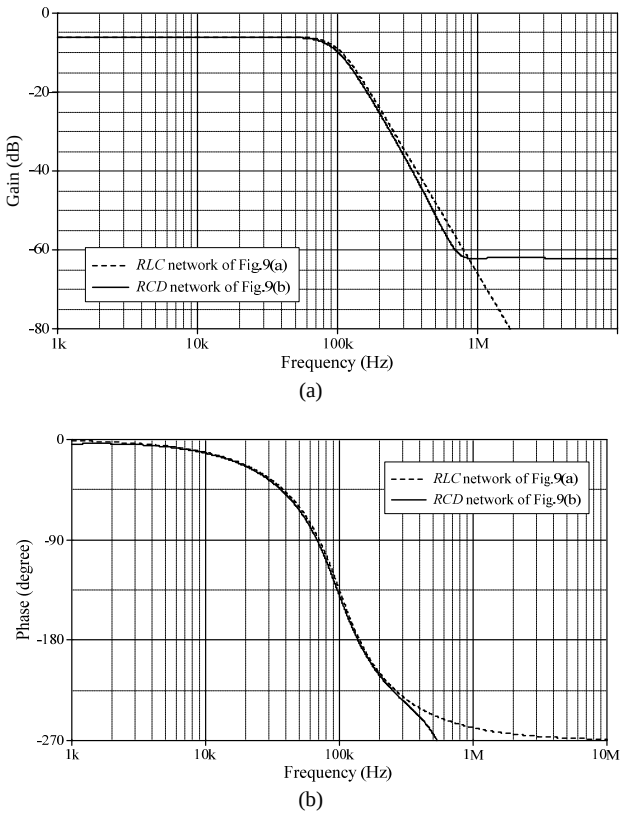

Fig. 10. Simulated frequency responses of the filters in Fig.9.
(a) gain responses (b) phase responses.

VII. Conclusion

The simple realization scheme of an electronically tunable grounded FDNC based on G_m-cell technique has been described. The FDNC realization circuit is constructed by only two grounded capacitors as passive elements, resulting in a resistorless structure and suitable for integration. No component matching is needed for its realization. The described FDNC circuit has been shown to be useful in realizing a grounded FDNR. The element values of the realized FDNC and FDNR can be tuned electronically through the external bias currents. The functionalities of the realized FDNC and FDNR are demonstrated on the third-order highpass and lowpass LC ladder filters. Simulation results with TSMC 0.35-μm CMOS technology have been provided and the obtained results confirm well the theory.

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