Electronically Tunable Floating Capacitance Multiplier Using FB-VDBAs

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***Abstract*—This paper presents a resistorless realization of the floating capacitance multiplier circuit based on using full-balanced voltage differencing buffered amplifiers (FB-VDBAs) as active components. The proposed floating capacitor is composed of only two FB-VDBAs and a single grounded capacitor, without requiring an additional passive resistor. The resulting equivalent capacitance value is electronically tunable through the transconductances of the FB-VDBAs. An application of the proposed tunable floating capacitor in realizing the second-order active bandpass filter is also demonstrated. PSPICE simulation results have been included to confirm the theoretical prediction.**

***Index Terms*— Full-Balanced Voltage Differencing Buffered Amplifier (FB-VDBA), floating capacitance multiplier, immittance simulator, tunable circuits and devices,**

I. Introduction

In the design of integrated circuit technologies, it is still a limiting impractical to fabricate large-valued physical capacitors because of occupied chip area. Therefore, the design of a floating capacitance multiplier circuit is advantageous from very large-scale integration (VLSI) implementation point of view. This is due to the well-known fact that the capacitance simulator circuit helps to obtain higher equivalent integrated capacitors, and escape from the use of a large silicon chip area [1]. Consequently, several capacitance multiplier implementations using various modern active elements are available in the open technical literature [2]-[14]. However, they need either two of more active devices or more than one passive element for their realizations [2]-[13], and also use some floating passive components [3]-[7], [14]. Moreover, they employ any external passive resistors [3]-[11], [14]. It should be noted that the circuit using a minimum number of active and passive elements is important from the point of view of VLSI implementation, power consumption, cost and area on the chip. Recently, the new active element called full balanced voltage differencing buffered amplifier (FB-VDBA) was introduced [15]. Many interesting applications of FB-VDBA, especially in analog signal processing and signal generation areas, were also introduced in [16]-[19], to demonstrate the usefulness and easy implementation in fully-balanced structures.

This paper presents an alternative configuration for realizing the floating capacitance multiplier topology. The proposed capacitor is generated with only two FB-VDBAs and one grounded capacitor, accordingly, it is a canonical structure and quite suitable for integrated circuit design. The equivalent capacitance value (C_{eq}) of the synthetic floating capacitor can be adjusted electronically through the adjustment of the FB-VDBA transconductance parameters. As an illustrative example, the usability of the realized floating capacitance simulator has been demonstrated on the design of an active second-order *RLC* bandpass filter. Computer simulation results are performed to verify the workability of the designed simulator circuit and its application.

II. Basic Concept of the FB-VDBA

The circuit representation and schematic symbol of the FB-VDBA are shown in Fig.1. As shown, the device has a pair of high-impedance differential voltage inputs (p and n), and a pair of high-impedance current outputs (z+ and z-) and low-impedance outputs of voltage buffers (w+ and w-). The terminal relations of the FB-VDBA in Fig.1 can be characterized by the following matrix equation [15]-[16]:

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ v_{w+} \\ v_{w-} \end{bmatrix} = \begin{bmatrix} g_m & -g_m & 0 & 0 \\ -g_m & g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \\ v_{z+} \\ v_{z-} \end{bmatrix} \quad (1)$$

where the parameter g_m implies the transconductance gain of the FB-VDBA. In general, it is possible to control the g_m-value electronically through the external supplied current or voltage.

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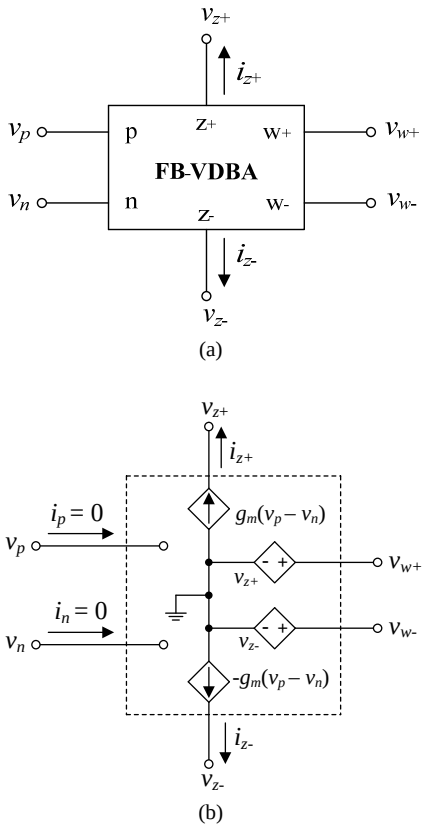


Fig. 1. FB-VDBA
(a) circuit diagram (b) schematic symbol.

III. Proposed Floating Capacitance Multiplier

The proposed floating capacitance multiplier circuit using FB-VDBAs as active elements is shown in Fig.2. The proposed capacitance simulator is constructed by two FB-VDBAs and one grounded capacitor without needing external passive resistors. The resulting structure is therefore canonical and preferable to further monolithic implementation point of view. Routine circuit calculation of the circuit in Fig.2 yields the following input impedance :

$$Z_{in} = \frac{v_1 - v_2}{i_1} = \frac{1}{s\left(\frac{C_1 g_{m2}}{g_{m1}}\right)} = \frac{1}{sC_{eq}} \qquad (2)$$

where g_{mi} denotes the transconductance value of i-th FB-VDBA (i = 1, 2). The above relation clearly indicates that the proposed simulator circuit simulates a tunable floating capacitor with an equivalent capacitance (C_{eq}) :

$$C_{eq} = \frac{C_1 g_{m2}}{g_{m1}} \qquad (3)$$

It is important to note from (3) that the C_{eq}–value obtained from the realized circuit is adjustable electronically by controlling the ratio of g_{m2}/g_{m1}.

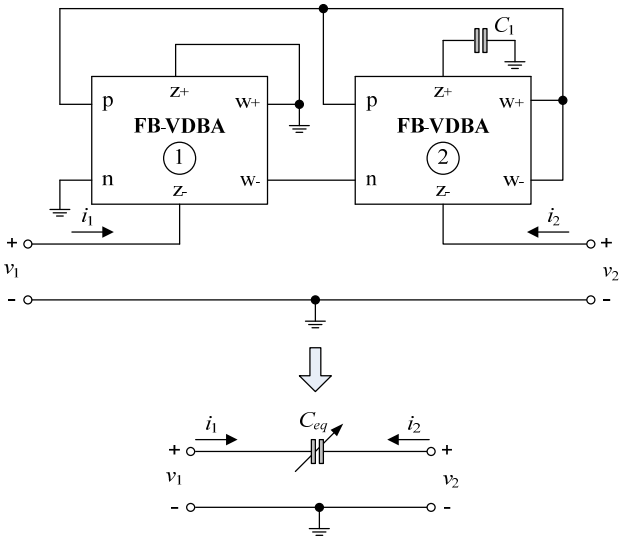


Fig. 2. Proposed electronically tunable floating capacitance multiplier circuit using FB-VDBAs.

IV. Simulation Results and Discussions

The performance verification of the proposed capacitance multiplier circuit in Fig.2 has been demonstrated through the PSPICE program simulation. For this purpose, the BiCMOS FB-VDBA structure given in Fig.3 was simulated with standard 0.35-μm BiCMOS process parameters [20]. The aspect ratios (W/L in μm/μm) of the transistors were provided as : 14/0.7 and 56/0.7 for M_1-M_2 and M_3-M_{10}, respectively. The circuit was simulated with DC power supply voltages equal to +V = -V = 1 V and bias current I_A = 25 μA.

From the schematic diagram of Fig.3, the input stage of the FB-VDBA mainly consists of input transistors (M_1-M_2 and Q_1-Q_4) and current mirror transistors (Q_5-Q_7, Q_8-Q_{10}, Q_{11}-Q_{12} and Q_{13}-Q_{14}), whereas the output stage is performed by transistors M_3-M_6 and M_7-M_{10} for providing the terminals w+ and w-, respectively. Consequently, the effective small-signal effective transconductance gain (g_m) of the FB-VDBA derived from the input stage can be derived in a fashion similar to that for the all bipolar version [21], giving :

$$g_m = \frac{I_B}{V_T} \qquad (4)$$

where $V_T \cong$ 26 mV at 27°C is the thermal voltage. It may be easily visualized that the g_m-value is tunable linearly and electronically by an external DC bias current I_B.

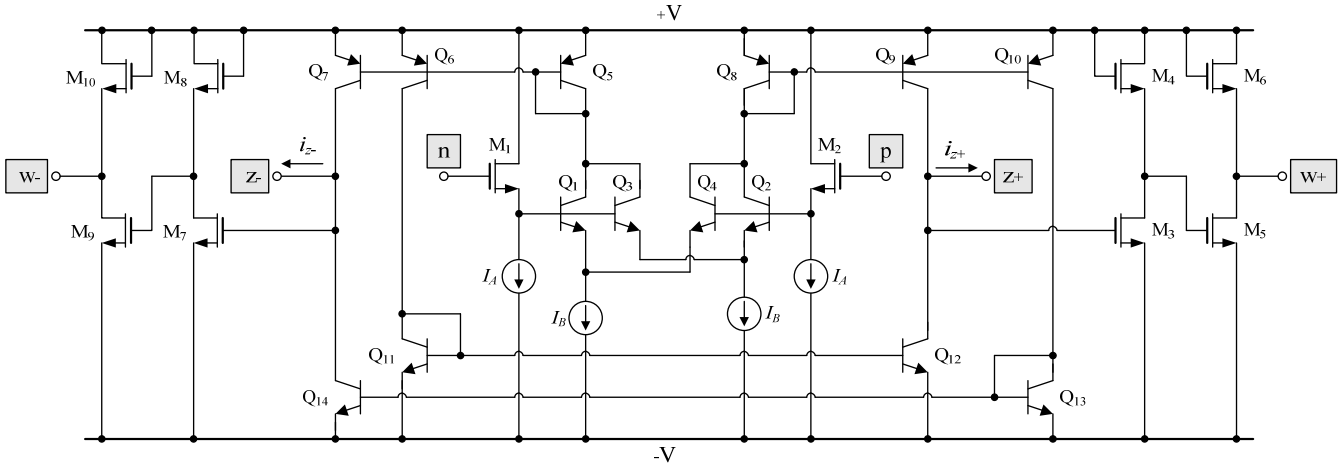


Fig. 3. BiCMOS realization of the FB-VDBA used in simulations.

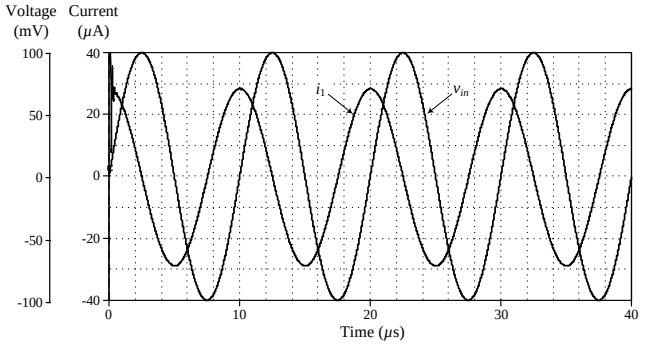
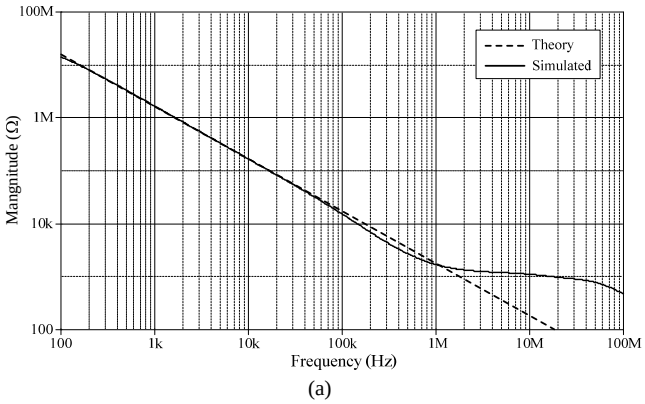
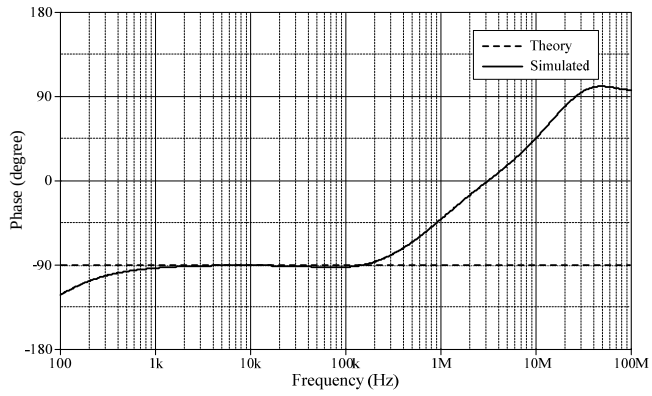


Fig. 4. Simulated transient waveforms for v_{in} and i_1 of the proposed synthetic floating capacitor in Fig.2.



(a)



(b)

Fig. 5. Simulated frequency characteristics for Z_{in} of the proposed synthetic floating capacitor in Fig.2.
(a) magnitude characteristic (b) phase characteristic.

Fig.4 shows the simulated time-domain responses for the differential input voltage v_{in} , i.e. $v_{in} = v_1 - v_2$, and the input current i_1 of the proposed floating capacitance simulator in Fig.2 with the following active and passive components : C_1 = 0.1 nF and $g_{m1} = g_{m2} \cong 1.92$ mA/V ($I_{B1} = I_{B2} \cong 50$ μA), resulting in C_{eq} = 0.1 nF. The resulting waveforms clearly indicate that the current i_1 leads the voltage v_{in} by 89°. The simulated frequency characteristics of the input impedance Z_{in} of the proposed capacitor along with the theoretical responses are also plotted in Fig.5. It can be seen that a good correspondences between the values can be observed for the operating frequency range roughly 1 kHz-100 kHz, i.e., error within 5%.

In order to demonstrate the electronic tuning of the C_{eq}-value, the simulations are performed with three different values of g_{m1}, i.e. $g_{m1} \cong 3.84$ mA/V, 1.92 mA/V, 1.28 mA/V, ($I_{B1} \cong 100$ μA, 50 μA and 33 μA). This adjustment results in C_{eq} = 0.05 nF, 0.1 nF and 0.15 nF, respectively. Fig.6 shows the magnitudes of the proposed synthetic floating capacitor in Fig.2 for various values of g_{m1} and an ideal capacitor against frequency. From Fig.6, it can be observed that the values of C_{eq} can be changed electronically through adjusting g_{m1}, as expected.

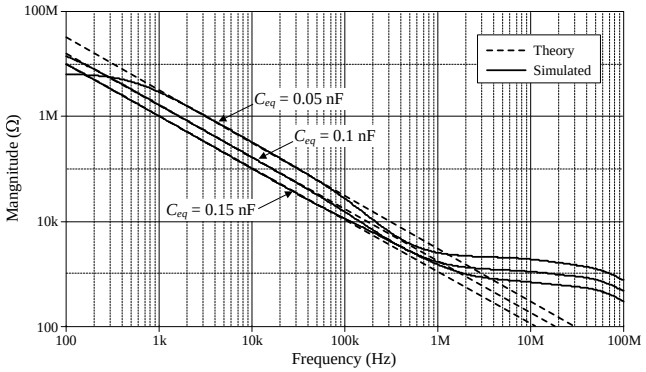


Fig. 6. Magnitude-frequency characteristics for Z_{in} of Fig.2 with various values of g_{m1}.

V. Application Example

To illustrate an application of the proposed simulator circuit, the second-order *RLC* bandpass filter as shown in Fig. 7 is realized and simulated. The voltage transfer function is given by :

$$\frac{V_o(s)}{V_{in}(s)} = \frac{sRC_{eq}}{s^2LC_{eq} + sRC_{eq} + 1} \tag{5}$$

and its natural angular frequency is obtained as :

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{LC_{eq}}} \tag{6}$$

As an example, the filter of Fig.7 was realized with R = 1.6 kΩ and L = 6.8 mH. For this purpose, the C_{eq} was realized by using the proposed floating capacitance multiplier in Fig.2 with C_1 = 0.1 nF and $g_{m1} = g_{m2} \cong 1.92$ mA/V, thus an equivalent capacitance of $C_{eq} \cong 0.1$ nF is obtained which results in f_o = 193 kHz. The frequency responses of the bandpass filter in Fig. 7 are shown in Fig.8. It appears, thus, that the simulated and ideal values are in good agreement.

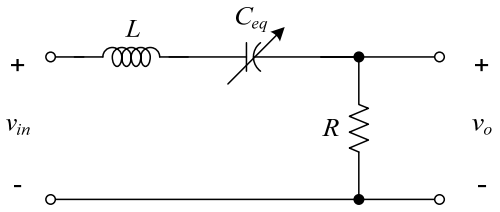


Fig. 7. Second-order RLC bandpass filter realized with the proposed synthetic floating capacitor in Fig.2.

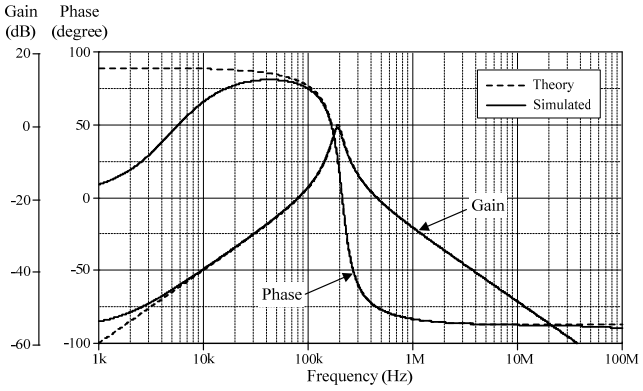


Fig. 8. Theoretical and simulated frequency responses of the bandpass filter in Fig.7.

In addition, to further demonstrate the electronic controllability of the proposed floating capacitor, the value of C_{eq} in Fig.7 has been respectively varied to 0.05 nF, 0.1 nF and 0.15 nF, by tuning $g_{m1} \cong 3.84$ mA/V, 1.92 mA/V, 1.28 mA/V, while keeping g_{m2} constant at 1.92 mA/V. This tuning leads to obtain $f_o \cong$ 270 kHz, 193 kHz and 156 kHz, respectively. Simulation results of the bandpass filter responses with three different values of C_{eq} are given together with the responses from the ideal circuit in Fig.9. For this filter, there is small deviation between ideal and simulated responses in the low-frequency region of the frequency response.

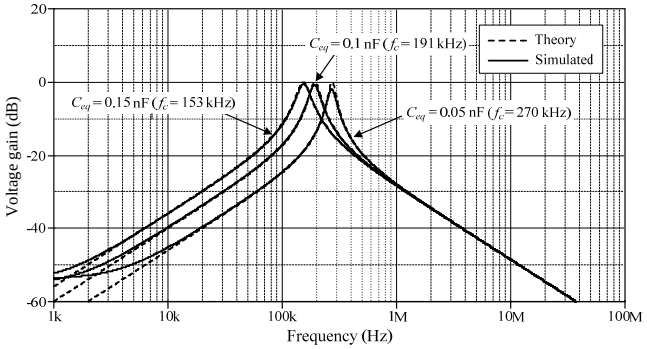


Fig. 9. Theoretical and simulated gain responses of the bandpass filter in Fig.7 with electronic tuning of the C_{eq}-value.

VI. Conclusion

In this paper, a circuit configuration for actively simulation of the floating capacitance multiplier is proposed. The proposed simulator employs only two FB-VDBAs and one grounded capacitor, which results in simple and resistorless topology as well as attractive for further integration. Its equivalent capacitance values can be adjusted electronically through the transconductance parameters of the FB-VDBAs. An application example of the proposed circuit is demonstrated on the second-order *RLC* bandpass filter. The performances of the proposed circuit along with its application are also discussed and verified by PSPICE simulations using standard 0.35-μm BiCMOS technology.

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