Digital Noncoherent Demodulator of Four-position Differential Phase Shift Keyed Signals

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***Abstract*—There is introduced the fast digital noncoherent demodulator of high-frequency differential quadrature phase shift keyed signals that provides the minimum number of arithmetic operations over the carrier frequency period. Thus, for the first time, for digital noncoherent demodulators the problem is solved of increasing the speed of high-frequency signal processing in common data transmission systems, for example, in TETRA, PHS, SDMA, IEEE 802.11 and IEEE 802.11b, ZigBee, etc. These and other data transmission systems operate at low power consumption, and this would need to minimize FPGA resources required for the implementation of the demodulation of high-frequency signals. This can be achieved by minimizing the appropriate computational costs in processing the signals. For this purpose the algorithm is presented that allows fast processing of the signal samples with a subsequent decision on the received symbol. The properties of the responses of the demodulator and its frequency-selective properties are also demonstrated. There is studied the influence of phase and frequency mismatch on the performance of the demodulator. The expressions are found for the symbol-error probability for the case when the information signal is distorted by band Gaussian noise. It is proved that the considered algorithm provides optimal signal extraction against broadband interferences and demonstrates potential interference immunity in the presence of Gaussian noises. It is established that the obtained theoretical results are confirmed by statistical simulation. The implementation of the proposed demodulation algorithm based on the field programmable gate arrays makes it possible to design highly efficient digital demodulators of high-frequency signals while utilizing minimal FPGA resources.**

***Index Terms*—Differential phase keying, digital demodulation, noncoherent processing, phase mismatch, frequency mismatch, interference immunity, bit-error probability**

I. Introduction

The differential phase shift keyed (DPSK) signal is a sequence of information symbols of the form of $s(t) = S\sin(2\pi f_0 t + \psi)$ with the amplitude S, the frequency f_0, the initial phase ψ and the duration of $N = 2^n$ periods T_0, where $T_0 = 1/f_0$ and n is an integer [1-5]. The transmitted discrete messages are determined by the phase shift φ between the received information symbol and the previous one. For a four-position DPSK (DPSK4 or DQPSK) the value of φ can be 0, $\pi/2$, π, $3\pi/2$ or shifted relative to these values by $\pi/4$ ($\pi/4$ DPSK4 or $\pi/4$ DQPSK). The DPSK application eliminates the phenomenon of the "sign ambiguity" of the phase shift keyed signal demodulator [1].

Noncoherent (quadrature) processing of DPSK signals makes it possible to avoid applying the phase synchronization between the received signal and the demodulator. It simplifies demodulator practical implementation, but leads to an interference immunity reduction.

The common noncoherent four-position DPSK signal demodulators are focused on analog implementation. In this connection, the development of fast digital noncoherent high-frequency DPSK signal demodulators that can provide a minimal number of simple arithmetic operations over the high-frequency signal period together with the potential interference immunity is of great interest and is highly relevant for the development of the modern communication systems. The introduced demodulator can be used in digital communication systems while stringent requirements are made for both power consumption and mass and dimensional characteristics consistent with the TETRA, PHS, SDMA, IEEE 802.11 and IEEE 802.11b, ZigBee standards and the like.

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II. Noncoherent Four-position DPSK Signal Demodulation

Digital processing involves the input signal sampling by the analog-to-digital converter. In order to achieve fast signal processing [6], there is proposed the digitization procedure with the sampling frequency $f_Q = 4f_0$ as it is shown in Fig. 1. Here s_{1i}, s_{2i}, s_{3i}, s_{4i} marked by points are the signal samples within *i*-th processed period.

Generation of the four samples over each signal period T_0 with their separation into even and odd pairs shifted in time by a quarter of the period or by 90^0 by the phase, as it is described in [7, 8], makes it possible to implement the quadrature channels of digital phase shift keyed signal processing. With the results of the previous studies [7, 8] in mind, the block diagram of the digital noncoherent four-position DPSK signal can be presented as it is shown in Fig. 2.

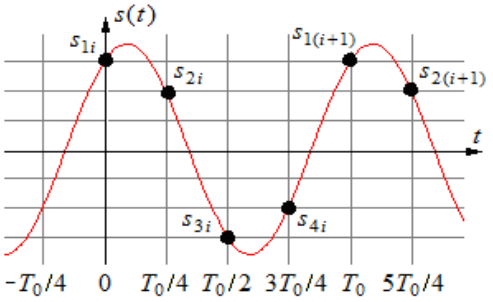

Fig. 1. Time diagram of the DPSK signal sampling.

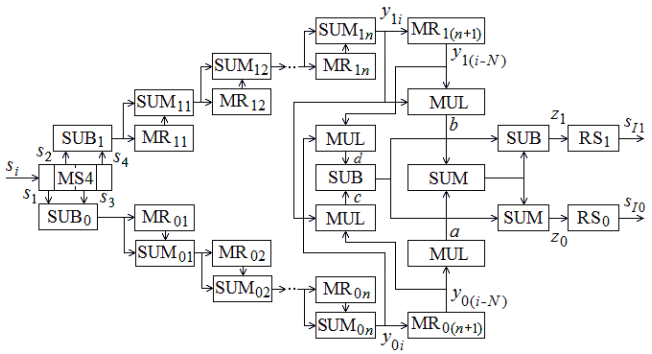

Fig. 2. The block diagram of the demodulator.

In SUB_0 subtractor, the difference $(s_{1i} - s_{3i})$ is formed between the odd samples s_{1i} and s_{3i} of the processed *i*-th period and, then, in SUM_{01} summator, it is summarized with the like value $(s_{1(i-1)} - s_{3(i-1)})$ calculated in the previous period and stored into multibit one cell shifter MR_{01}. After that, in MR_{01}, the value $(s_{1(i-1)} - s_{3(i-1)})$ is replaced by the new value $(s_{1i} - s_{3i})$. The sum $(s_{1i} - s_{3i}) + (s_{1(i-1)} - s_{3(i-1)})$ from SUM_{01} is added into SUM_{02} with the sum $(s_{1(i-2)} - s_{3(i-2)}) + (s_{1(i-3)} - s_{3(i-3)})$ calculated in the $(i-2)$-th period and stored into multibit three-cell shifter MR_{02}. After that, the first of the sums specified above is stored in the first MR_{02} cell shifting the data poked earlier. Further, similar calculations are carried out of which the response y_{0i} of the first quadrature channel is formed at the summator SUM_{0n} output. Under $i \geq N$, the value y_{0i} is the sum of the differences of odd samples $(s_{1i} - s_{3i})$ for the N of the last received signal periods:

$$y_{0i} = \sum_{j=0}^{N-1} \left(s_{1(i-j)} - s_{3(i-j)} \right). \tag{1}$$

The value y_{0i} are written into the *N* cell shifter $MR_{0(n+1)}$, while at the $MR_{0(n+1)}$ output the value $y_{0(i-N)}$ appears obtained earlier and is equal to

$$y_{0(i-N)} = \sum_{j=N}^{2N-1} \left(s_{1(i-j)} - s_{3(i-j)} \right). \tag{2}$$

The processing of even samples s_{2i} and s_{4i} is similarly carried out. As a result, at the SUM_{1n} output the response of the second quadrature channel is formed as follows

$$y_{1i} = \sum_{j=0}^{N-1} \left(s_{2(i-j)} - s_{4(i-j)} \right), \tag{3}$$

while the value $y_{1(i-N)}$ equal to

$$y_{1(i-N)} = \sum_{j=N}^{2N-1} \left(s_{2(i-j)} - s_{4(i-j)} \right) \tag{4}$$

is popped from the *N* cell shifter $MR_{1(n+1)}$.

In order to form a decision on the received symbol, in MUL multipliers the products are calculated of the form of

$$\begin{cases} a = y_{0i} y_{0(i-N)}, & b = y_{1i} y_{1(i-N)}, \\ c = y_{1i} y_{0(i-N)}, & d = y_{0i} y_{1(i-N)}. \end{cases} \tag{5}$$

And then, by the SUM summators and the SUB subtractors the values

$$\begin{cases} z_0 = a + b + c - d = \\ = y_{0i} y_{0(i-N)} + y_{1i} y_{1(i-N)} + y_{1i} y_{0(i-N)} - y_{0i} y_{1(i-N)}, \\ z_1 = a + b - c + d = \\ = y_{0i} y_{0(i-N)} + y_{1i} y_{1(i-N)} - y_{1i} y_{0(i-N)} + y_{0i} y_{1(i-N)} \end{cases} \tag{6}$$

are formed. Based on the values (6), the decision on the received four-position information symbol $s_I = s_{I1} s_{I0}$ is made in the resolvers (digital comparators) RS_0 and RS_1 by the comparison of z_0 and z_1 with zero as it is specified in Table 1. This decision may be 00, 01, 10, 11.

In Fig. 3, the dependences of the normalized responses $y_0/2NS$ and $y_1/2NS$ of the quadrature channels upon the

TABLE I
THE DEMODULATOR RESPONSES AND THE DECISION RULE ON THE RECEIVED FOUR-POSITION INFORMATION SYMBOL

v	z_0	z_1	z_0 sign	z_1 sign	s_I
0	$(2NS)^2$	$(2NS)^2$	$z_0>0$	$z_1>0$	00
1	$-(2NS)^2$	$(2NS)^2$	$z_0<0$	$z_1>0$	01
2	$-(2NS)^2$	$-(2NS)^2$	$z_0<0$	$z_1<0$	10
3	$(2NS)^2$	$-(2NS)^2$	$z_0>0$	$z_1<0$	11

normalized number i/N of a current information symbol are respectively shown by solid and dashed lines. These curves are obtained by means of simulations, for the case when $N=256$ and interferences are absent. In Fig. 4, the similar dependences of the normalized responses $z_0/(2NS)^2$ and $z_1/(2NS)^2$ of the demodulator are drawn. As it can be seen, the graphs in Figs. 3, 4 have the similar rectilinear form reflecting the optimal signal samples accumulation [9] that is practically implemented in the proposed demodulator. The parabolic shape of curves in Fig. 4 is caused by the multiplication of the responses of the quadrature channels, and it helps to make decision concerning the received symbol.

In presence of interferences, the distortions of the demodulator output signals are observed. As an example, in Fig. 5 the time diagrams of the normalized responses $z_i/(2NS)^2$, $i=0,1$ of the demodulator are plotted, for the case when the useful signal is received against band

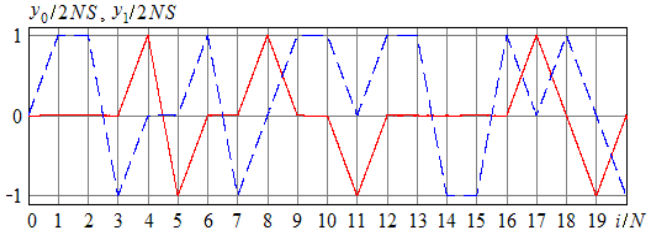

Fig. 3. The time diagrams of the quadrature channel responses in the absence of interferences: $y_0/2NS$ – solid line; $y_1/2NS$ – dashed line.

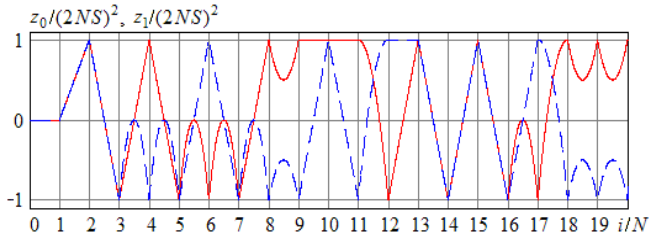

Fig. 4. The time diagrams of the demodulator responses in the absence of interferences: $z_0/(2NS)^2$ – solid line; $z_1/(2NS)^2$ – dashed line.

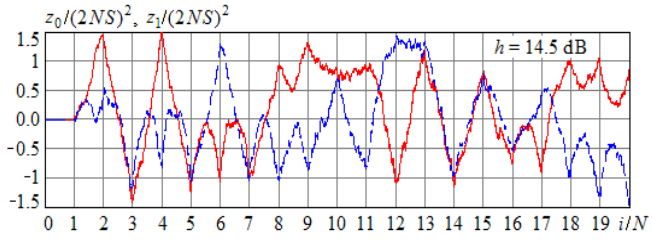

Fig. 5. Time diagrams of the demodulator responses when receiving the signal against band Gaussian noise: $z_0/(2NS)^2$ – solid line; $z_1/(2NS)^2$ – dashed line.

Gaussian noise and the output voltage signal-to-noise ratio is 14.5 dB. It is obvious that the distortions of the demodulator responses increase with the interference level, and, therefore, the probability of error symbol reception at the demodulator output therefore increases too.

It must be emphasized that the proposed optimal processing of the radio signal at a high intermediate frequency of the receiver reduces the effect of its nonlinear transformations in the low-frequency region on the interference immunity of demodulation.

III. DEMODULATOR RESPONSE PROPERTIES

When interferences are absent and the sampling frequency $f_Q = 4f_0$, at the information symbol end points the quadrature channel responses y_{0i}, y_{1i} take the values

$$y_{0i} = 2NS\cos\varphi, \qquad y_{1i} = 2NS\sin\varphi, \tag{7}$$

while for the previous symbol one has

$$y_{0(i-N)} = 2NS\cos(\varphi + v\pi/2), \quad y_{1(i-N)} = 2NS\sin(\varphi + v\pi/2), \tag{8}$$

Here φ is the initial phase of the input signal, $v = 0,1,2,3$ is the decimal equivalent of the information signal s_I (see Table 1). From (7), (8) it can be seen that the magnitudes of the quadrature channel responses depend on the initial phase of the input signal.

By substituting (7) and (8) in (5), one gets

$$\begin{cases} a = y_{0i}y_{0(i-N)} = (2NS)^2\cos\varphi\cos(\varphi + v\pi/2), \\ b = y_{1i}y_{1(i-N)} = (2NS)^2\sin\varphi\sin(\varphi + v\pi/2), \\ c = y_{1i}y_{0(i-N)} = (2NS)^2\sin\varphi\cos(\varphi + v\pi/2), \\ d = y_{0i}y_{1(i-N)} = (2NS)^2\cos\varphi\sin(\varphi + v\pi/2), \end{cases}$$

whence it follows that

$$\begin{cases} a + b = y_{0i}y_{0(i-N)} + y_{1i}y_{1(i-N)} = (2NS)^2\cos(v\pi/2), \\ c - d = y_{1i}y_{0(i-N)} - y_{0i}y_{1(i-N)} = -(2NS)^2\sin(v\pi/2), \end{cases} \tag{9}$$

By applying (9) in (6), one obtains the following relations

$$\begin{cases} z_0 = a + b + c - d = (2NS)^2[\cos(v\pi/2) - \sin(v\pi/2)], \\ z_1 = a + b - c + d = (2NS)^2[\cos(v\pi/2) + \sin(v\pi/2)]. \end{cases} \tag{10}$$

According to (9), (10), the values of both $(a+b)$, $(c-d)$ and z_0, z_1 do not depend on the initial phase of the received signal, and they are determined by the phase difference of neighboring information elements. In the absence of interferences the values z_0 and z_1 are equal to $\pm(2NS)^2$ for all the combinations of information symbols, as it is shown in Table 1.

If the noise with dispersion σ_n^2 is present at the input of the demodulator, then the responses of the quadrature channels y_{0i} and y_{1i} are the random variables with mean values (7) and the same dispersions

$$\sigma_y^2 = 2N\sigma_n^2. \tag{11}$$

Here it is taken into account that in the channels y_{0i} and y_{1i}, $2N$ samples are summed up of the additive mix of signal and noise. If the input noise is non-Gaussian, then, according to the central limit theorem, the normalization of the noise components at the outputs of the quadrature channels occurs due to the multiple summation as it follows from (1)-(4).

IV. Estimation of Demodulator Interference Immunity

Let us present the demodulator responses z_0 and z_1 (10) in the following way

$$\begin{cases} z_0 = \left[\left(y_{0i} + y_{0(i-N)}\right)^2 + \left(y_{1i} + y_{1(i-N)}\right)^2 - \left(y_{1i} + y_{0(i-N)}\right)^2 - \left(y_{0i} - y_{1(i-N)}\right)^2\right]/2, \\ z_1 = \left[\left(y_{0i} + y_{0(i-N)}\right)^2 + \left(y_{1i} + y_{1(i-N)}\right)^2 - \left(y_{1i} - y_{0(i-N)}\right)^2 - \left(y_{0i} + y_{1(i-N)}\right)^2\right]/2. \end{cases}$$

Then for the decision rules $z_0 <> 0$ and $z_1 <> 0$ (Table 1), similarly to [1], one obtains the inequalities based on the quadratic forms of the quadrature channel responses:

$$\begin{cases} \left(y_{0i} + y_{0(i-N)}\right)^2 + \left(y_{1i} + y_{1(i-N)}\right)^2 <> \left(y_{1i} + y_{0(i-N)}\right)^2 + \left(y_{0i} - y_{1(i-N)}\right)^2, \\ \left(y_{0i} + y_{0(i-N)}\right)^2 + \left(y_{1i} + y_{1(i-N)}\right)^2 <> \left(y_{1i} - y_{0(i-N)}\right)^2 + \left(y_{0i} + y_{1(i-N)}\right)^2. \end{cases}$$

As it is well known, the probability density of the sum of squares of two normal random variables obeys the chi-square distribution with two degrees of freedom [10]. In view of the latter, the probability of error in one bit of the demodulation product (s_{I0} or s_{I1}) is equal to

$$p_{err} = \int_0^\infty w_\chi(x_1) \int_{x_1}^\infty w_\chi(x_2)\,dx_1 dx_2, \tag{12}$$

where $w_\chi(x_1)$ and $w_\chi(x_2)$ are the probability densities of the noncentral chi-square distribution with two degrees of freedom:

$$w_\chi(x_i) = \frac{1}{2\sigma_z^2} \exp\left(-\frac{x_i + \Delta_i}{2\sigma_z^2}\right) \mathrm{I}_0\left(\frac{\sqrt{x_i \Delta_i}}{\sigma_z^2}\right), \quad i = 1,2. \tag{13}$$

Here $\Delta_1 = (2NS)^2 \cos^2(\pi/8)$, $\Delta_1 = (2NS)^2 \sin^2(\pi/8)$ are the noncentrality parameters [1], $\sigma_z^2 = 2\sigma_y^2 = 4\sigma_n^2$ is the dispersion of the demodulator response determined by two information symbols (by $4N$ samples), $\mathrm{I}_0(x)$ is the modified zero-order Bessel function [11], and σ_y^2, σ_n^2 are defined from (11).

By substituting (13) in (12), after simple transformations by analogy with [1], for the error probability one gets

$$p_e = \mathrm{Q}(\alpha,\beta) - \exp\left(-h^2\right)\mathrm{I}_0\left(h^2/\sqrt{2}\right)/2, \tag{14}$$

where $\alpha = \sqrt{2}h\sin(\pi/8)$, $\beta = \sqrt{2}h\cos(\pi/8)$, $\mathrm{Q}(\alpha,\beta) = \int_\beta^\infty t \exp\left[-\left(\alpha^2 + t^2\right)/2\right]\mathrm{I}_0(\alpha t)\,dt$ is the Marcum function [12], and

$$h^2 = NS^2/\sigma_n^2 \tag{15}$$

is the power signal-to-noise ratio for a binary information symbol at the output of the demodulator.

The errors in the received symbol bits can be considered as independent, because the responses of the quadrature channels are orthogonal. Then the probability of erroneous demodulation of four-position DPSK signal is equal to

$$p_{e4} = 1 - (1 - p_e)^2, \tag{16}$$

where p_e is defined by the expression (14).

The dependence (16) of the error probability p_{e4} of noncoherent four-position DPSK signal demodulation upon the SNR h (15) is shown in Fig. 6 by upper solid line. The experimental p_{e4} values learned from the statistical simulation are drawn by points. By dashed line the similar theoretical dependence is drawn of the error probability p_{e2} for the case when noncoherent binary DPSK signal demodulation is used. When comparing the curves presented for the error probabilities p_{e2} and p_{e4}, it is taken into account that bit rate for the four position DPSK signal is two times higher than that of the binary DPSK signal with the same symbol duration. The resulting estimate of the probability of error indicates the optimality of the proposed technical solution [13].

The lower solid line in Fig. 6 represents the error probability p_{e4C} of coherent four-position DPSK signal demodulation. As it can be seen, in the coherent mode, interference immunity increases significantly. It is thus advisable to examine the possibility of using the second-order four-position differential phase-shift keying, which,

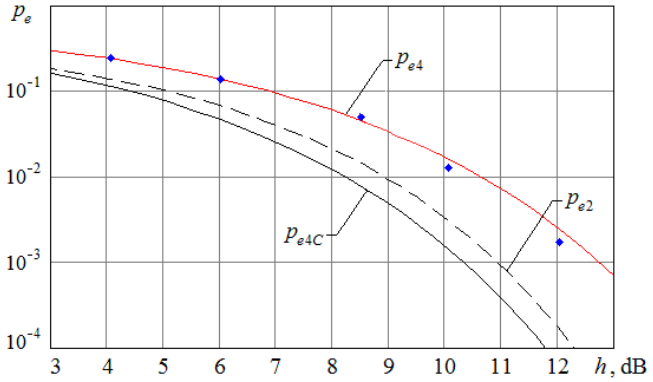

Fig. 6. The error probability.

according to [1], can permit interference immunity of incoherent demodulation to be closer to coherent one.

V. The Influence of Phase and Frequency Fluctuations

The resulting estimate of the error probability presupposes that the condition $f_Q = 4 f_0$ holds and the initial phase φ of the received signal is constant, since the demodulator responses (10) in this case do not depend on φ. If weak chaotic phase fluctuations with zero mean and root-mean-square value σ_φ occur, then they are being transformed into random fluctuations of the quadrature channel responses y_{0i}, y_{1i}. This in turn leads to increasing the noise level at the output of the demodulator and therefore the signal-to-noise ratio decreases. According to [4, 14], for binary differential phase-shift keying it is required to provide the values of σ_φ that are not greater than $0.2 \div 0.3$ radians, while for four-position differential phase-shift keying – the values of σ_φ should be lower by 2-3 times, respectively. Otherwise the error probability increases abruptly, especially, in the domain of its small values.

The deviation of the actual signal frequency f_0 from the design value $f_0' = f_Q/4$ by the bias Δf results in the demodulator response the signal component decreasing and that also leads to the signal-to-noise ratio decreasing. As an example, in Fig. 7 the dependence is shown of the error probability on the relative mismatch δ resulting from simulation. The mismatch δ is defined as

$$\delta = \Delta f / f_0 = (f_0' - f_0)/ f_0 .$$

From Fig. 7 it follows that the relative frequency mismatch values should not exceed 10^{-5}. It imposes the corresponding requirements to both the oscillator frequency stability and the Doppler signal frequency shift. In this regard, it is relevant to study and to develop the digital correlation demodulators of second-order DPSK signals [1], since such signals are invariant to the demodulator frequency mismatch.

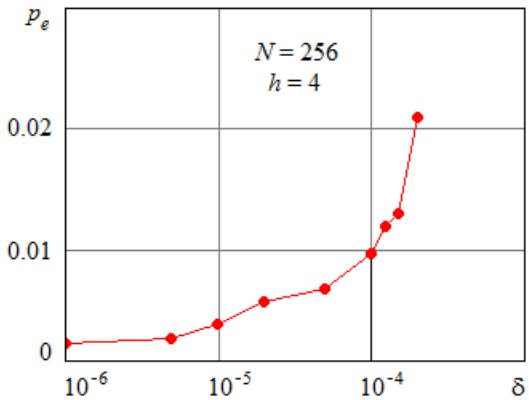

Fig. 7. The influence of the frequency mismatch.

VI. Hardware Implementation

The considered demodulator can be effectively implemented by means of the modern field programmable gate arrays (FPGAs), including, for example, the FPGA Spartan-6 or Virtex-5 families [15, 16]. These FPGAs provide signal processing at the frequencies of the input signal up to 50-100 MHz, subject to the availability of an appropriate analog-to-digital converter. For the sampling frequency $f_Q = 200$ MHz the required FPGA power is 40-80 mW.

VII. Conclusion

The introduced fast digital algorithms for the noncoherent demodulation of the four position DPSK signals require the minimum number of arithmetic operations over carrier period (that is, minimum hardware resources for its implementation based on the modern FPGAs). By simulation methods, the properties of the demodulator responses have been studied, and one demonstrates their time diagrams revealing an optimality of the signal samples accumulation procedure. The expressions for the probability of erroneous reception can be found when the useful signal is distorted by band Gaussian noise. From the comparison of these expressions with those for the optimal demodulators, one can prove that the introduced algorithms provide potential interference immunity. There have been estimated the influence that both the phase fluctuations of the received signal and the deviation of its carrier frequency from the expected value have on the demodulator performance. One can see that the demodulator is operable and efficient in real conditions. The presented theoretical results are corroborated by the corresponding experimental data found during the simulation. The possibility of implementing the proposed demodulator by means of the FPGA is stated, and that minimal hardware FPGA resources can then be required is also confirmed. This makes it possible to design highly efficient data transmission equipment with a significantly reduced power consumption.

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