# Hardware Implementation of the Cascaded H-Bridge Inverter using ARM Cortex M4 Microcontroller

Mahmadasraf A. Mulla, *Senior Member, IEEE and Member, IAENG*

*Abstract* — **A multilevel inverter is preferred over other power electronic converters for its advantages like low switching power loss, lesser harmonics, and reduced stress on switches. Cascaded H-Bridge (CHB) topology of the multilevel inverter is more popular because of its modular arrangement and non requirement of balancing or pre-charging of capacitors. In this paper, a constant voltage to frequency (*V/f*) ratio control of an induction motor is implemented using five-level CHB inverter. To obtain high-quality sinusoidal output current with reduced harmonics, multicarrier level shifted Pulse Width Modulation (PWM) scheme is implemented. The main aim of this work is to demonstrate easy realisation of CHB inverter using ST Microelectronics ARM Cortex M4 microcontroller STM32F407VG. For rapid development of control signals, the microcontroller is programmed using block sets in MATLAB/Simulink environment. Experimental investigations are carried out and results are presented to demonstrate easy implementation of CHB inverter applied for variable speed control of induction motor.**

*Index Terms* — **Cascaded H-bridge, Induction motor drive, Multicarrier SPWM, Multilevel inverter, Speed control.**

## I. Introduction

Because of unavailability of the variable frequency supply voltage, induction motor was mainly used for constant speed applications in the past. The advancement in semiconductor and power electronics technology has initiated the development of high-power semiconductor switches, which can be applied to achieve continuous, step-less, and smooth variation in motor speed. Conventionally, a two-level inverter is used for variable voltage variable frequency drive. In two-level inverter an output voltage is produced using voltage levels either $+V_{DC}$ or $-V_{DC}$, which improves the current produced by the voltage source inverter [1], [2]. Several new configurations of inverters are finding practical applications in recent times [3] – [5].

With an objective to reduce filter size, recent advancements in power electronics have led to increase in the level of the inverter. As an outcome in the last few decades, the significance of multilevel inverter (MLI) has increased. Among all multilevel converter configurations, the cascaded H-bridge (CHB) MLI is more popular because of its modular structure and operation without voltage balancing capacitors or clamping diodes. On the development front, generating gate pulses for large numbers of semiconductor switches used in the CHB MLI configuration is a major challenge [6], [7]. The control logic becomes more complex under unbalance and applications like micro-grid [8], [9]. Many implementations of CHB MLI are reported in the literature where the real-time platforms like dSPACE, OPAL-RT, Labview etc. are explored for generating gate pulses. These platforms ease the development cycle because of their connectivity with the MATLAB/Simulink environment for programming. However, it is not possible to migrate the developed MLI for the real-time applications [10], [11]. In industrial applications the Arduino and FPGA controllers are getting popular due to their strong software support [12] - [15].

Nowadays, 32-bit controllers are finding wide applications in the development of the control circuit because of their modularity and low cost. In 32-bit controller, generic ARM core-based digital signal controller are very much popular because of their rich peripheral support, math capabilities and support of DSP instructions. Normally they are programmed by writing code in C language and then using cross compiler to convert this source code to the controller specific binary instructions. Major development has taken place in microcontroller and there are many microcontrollers which offer model based programming using MATLAB/Simulink environment for rapid verification of research concepts. In this approach, the MATLAB model is first converted into C language code, which is further converted into processor specific binary codes using cross compilers. Finally, the generated binary code is dumped into the flash memory of the microcontroller. It offers all the rapid development advantages, that we can have with higher platforms with almost negligible cost [12]. The final outcome of such development can be directly used for real-time systems.

The major challenges in the development of CHB inverter are generation of control logic required for large numbers of semiconductor switches used in the power configuration. The ARM Cortex M4 32-bit processor is popular to address digital signal control which requires high-efficiency signal processing with ease-of-use and low cost. This study aims to demonstrate the capability of one such platform for such computational intensive real-time applications. In this development, for generating gate pulses, In Phase Disposition (IPD) level shifted Sinusoidal Pulse Width Modulation (SPWM) technique is implemented [16]. Realization of the required control logic using Waijung blocks is presented in details. For the completeness, the details of standard H-Bridge development are also included.

Author is with the Electrical Engineering Department, Sardar Vallabhbhai National Institute of Technology, Surat, Gujarat, India. (e-mail: mam@eed.svnit.ac.in, mamulla@ieee.org).

## II. System Configuration

In this section, the system configuration of five-level CHB inverter along with its control methods is reviewed.

### A. Cascaded H-bridge Multilevel Inverter

In CHB MLI, multiple cells of H-bridge are connected in series, to produce high AC voltages. Fig 1(a) shows a five-level CHB configuration. Two H-bridge cells are employed in each phase leg, in which each H-bridge cell is powered by isolated dc supply having E voltage. The output voltage waveform for a single-phase five-level CHB inverter is as shown in Fig. 1(b). Table I presents the switching table used for controlling the inverter [1], [16].

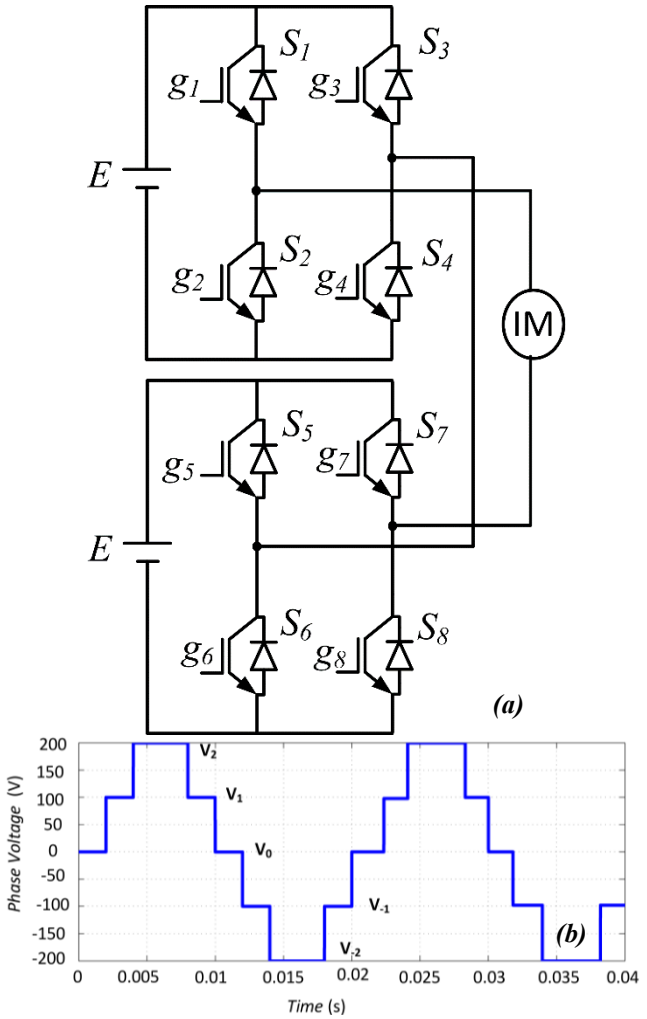


Fig. 1. Single Phase CHB Five-Level Inverter: (a) Power Configuration; and (b) Output Voltage Waveform.

TABLE I
Switching Table of CHB Five-Level Inverter

| Output Voltage | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ |
|---|---|---|---|---|---|---|---|---|
| $V_2 = 2E$ | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| $V_1 = E$ | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| $V_0 = 0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $V_{-1} = -E$ | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| $V_{-2} = -2E$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

### B. Pulse Width Modulation Technique

Conventional two-level SPWM technique can be applied to cascaded MLI by modifying carrier waveform. Two popularly used approaches are: (i) Level Shifted Carrier Wave, and (ii) Phase Shifted Carrier Wave [1]. This development uses, In Phase Disposition (IPD) level shifted Sinusoidal Pulse Width Modulation (SPWM) where-in all carrier wave has the same phase.

A level-shifted multicarrier SPWM requires *(L–1)* triangular carriers, where $L$ is numbers of levels. These carrier waves are vertically disposed of by providing a contiguous band. Amplitude and frequency of all the carriers are identical. The amplitude modulation index decides magnitude of output voltage and is defined as $m_a = V_m / V_c(L-1)$, where $V_m$ and $V_c$ are the peak amplitude of modulating wave and carrier wave, respectively. The frequency modulation index which decides switching frequency is given by, $m_f = f_c / f_m$, where, $f_c$ is the frequency of the carrier signal and $f_m$ is the frequency of a modulating signal.

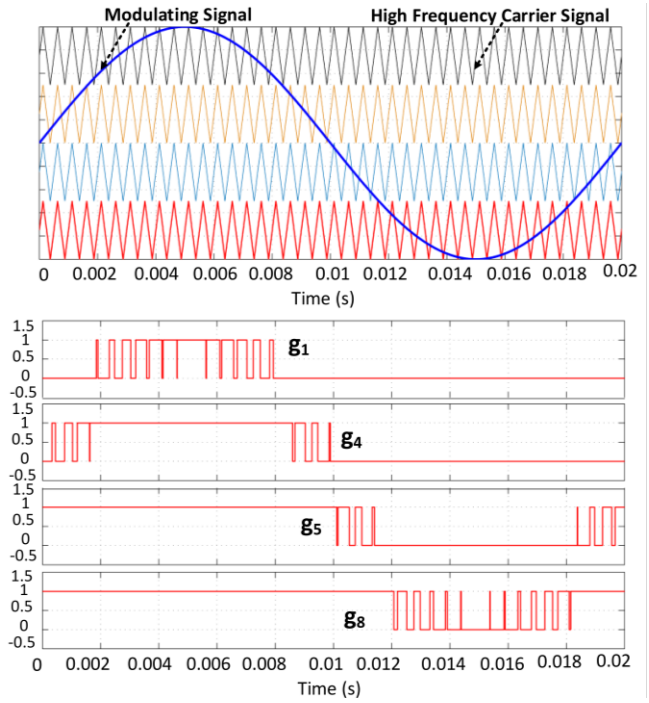


Fig. 2. Gate Pulse Generation using Level Shifted SPWM.

Figure 2 shows gate pulses for CHB inverter, generated by comparing a sinusoidal signal with four high-frequency carrier. The gate pulses generated by comparison with the top most carrier signal is given to switch $S_1$ and the complimented pulse is given to switch $S_2$. Similarly, pulses for $S_4$, $S_5$, $S_8$ are generated by comparision of second, third and forth carrier signal respectively; and its complement pulses are given to the switch $S_3$, $S_6$, $S_7$, respectively.

## III. Experimental Study, Results, And Discussion

The objective of this work is to demonstrate development cycle of complex five-level CHB inverter using generic core based 32-bit ARM Cortex microcontroller. First the level-shifted SPWM comparison for generating the gate pulses is implemented in the MATLAB/Simulink environment, which is then migrated for generating gate pulses. The photograph of the actual experimental setup is as shown in Fig. 3. Further sub-section presents the complete hardware and software details of the implementation.

### A. *Hardware Description of H-Bridge Card*

Standard three-phase H-Bridge card is used for the construction of CHB five-level inverter. The H-bridge card is constructed having optical isolation stage, IGBT driver circuit, and power circuit. Optical isolation section is constructed using IC 6N137. Switching pulses generated by controller are connected at the input of the isolator. The input side supply is also drawn from the digital controller input port pin power supply. An isolated power supply for the secondary side of the isolator is created on the H-Bridge card.

A three-phase bridge driver IC IR2130 is used. Lower side gate pulses (LO_1, LO_2, and LO_3) are directly generated by the bridge driver, however, for high side pulses (HO_1, HO_2 and HO_3) boots trapping mechanism is applied to lift the gate pulse level above the IGBT bridge emitter potential. Fig. 4(a) shows the detailed schematic of isolation and driver circuit.

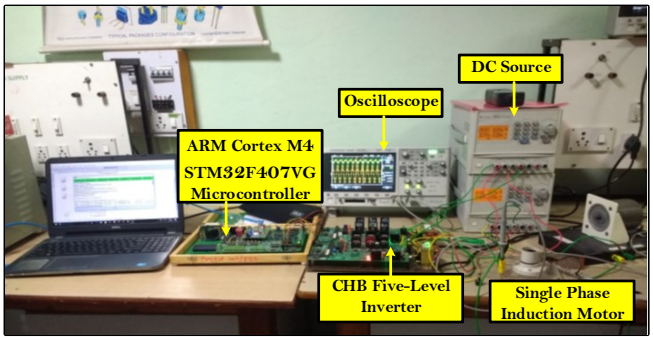


Fig. 3. Experimental Set-up Photograph.

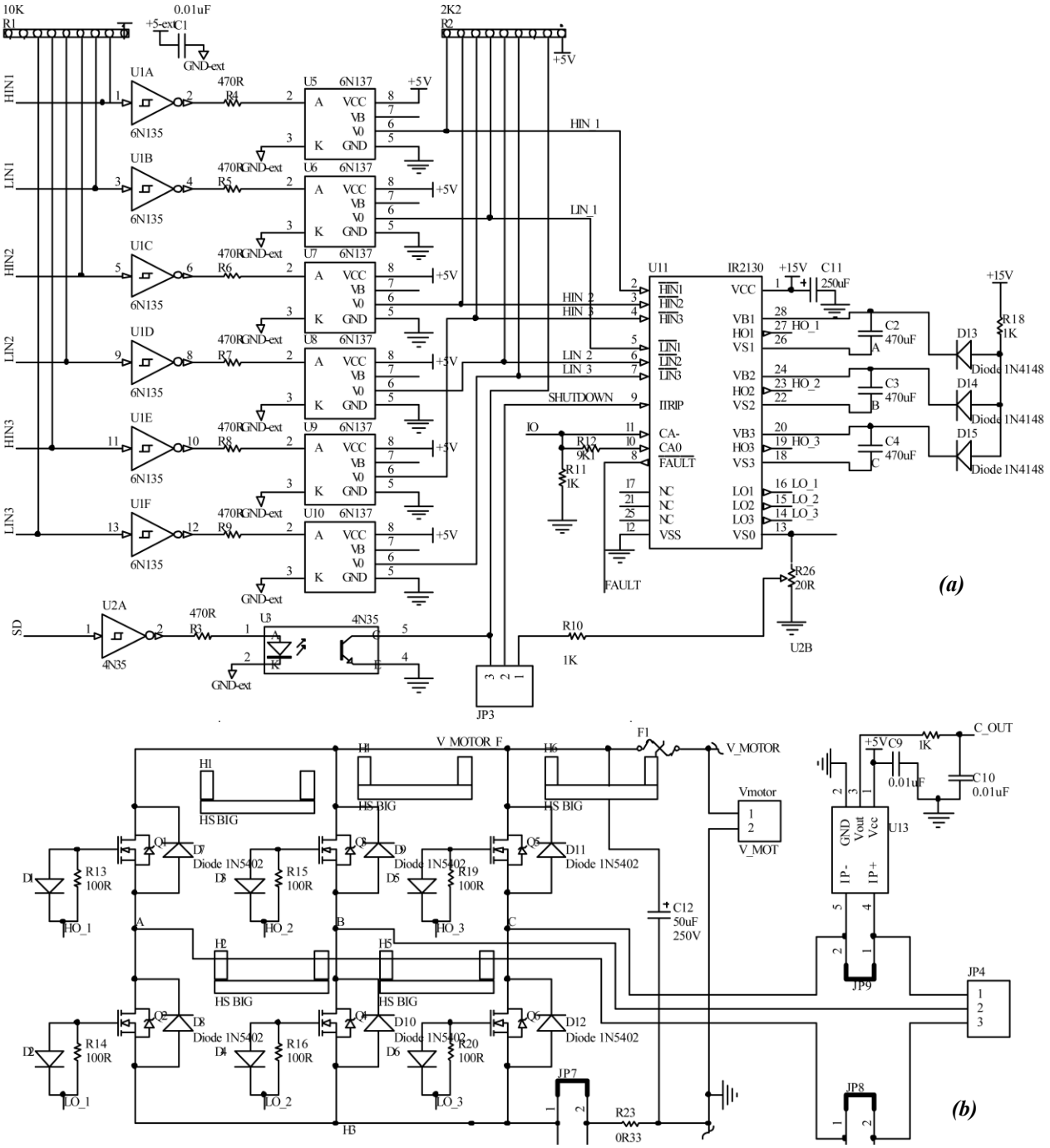


Fig. 4. Hardware details of H-Bridge: (a) Isolation plus driver circuit, and (b) Power circuit.

The power circuit is constructed by bridge connection of IGBTs STGW30NC120HD. The driver outputs are connected at the gate terminal of IGBT through the parallel combination of a gate resistor and fast recovery diode for fast turn-off. Fig. 4(b) shows the schematic of the power section of the H-Bridge card.

Two number of three-phase H-Bridge card are used to construct the power arrangement of CHB five-level inverter. Only two legs in each card are utilised in the power configuration accordingly four gate pulses are connected in each H-Bridge card.

### *B. Hardware Description of STM32F407 Microcontroller*

The microcontroller STM32F407VGT6 is based on a 32-bit RISC core, which supports ARM single precision data-processing instructions and data types owing to single precision Floating Point Unit (FPU). It enhances application security due to the implementation of a Memory Protection Unit (MPU) and a full set of DSP instructions. It also incorporates widespread range of improved I/Os and peripherals connected to two AHB buses, two APB buses, and a 32-bit multi-AHB bus matrix. All devices offer a low-power RTC, two DACs, three 12-bit ADC, two general-purpose 32-bit timers, and a true random number generator (RNG). It has twelve general-purpose 16-bit timers including two PWM timers, which are dedicated for motor control. The microcontroller also supports major standard and advanced communication interfaces.

The photograph of standard 32-bit microcontroller kit, which is based on STM32F407VG microcontroller is shown in Fig. 5. The controller port pins are buffered and terminated for the purpose of Digital Output (DO), Digital Input (DI), Analog Input (AI) and Analog Output (AO). There are total 20 DI, 36 DO, 09 AI and 02 AO pins available for external interfacing on this kit. For the user interface, the kit is having 2x16 LCD, 05 keys and 08 LEDs connected at different port pins. For communication, pins are allotted for a standard protocol like SPI, I2C, USART, and CAN. All pins are 5V tolerant and sink or source sufficient current to interface with another electronic stage.

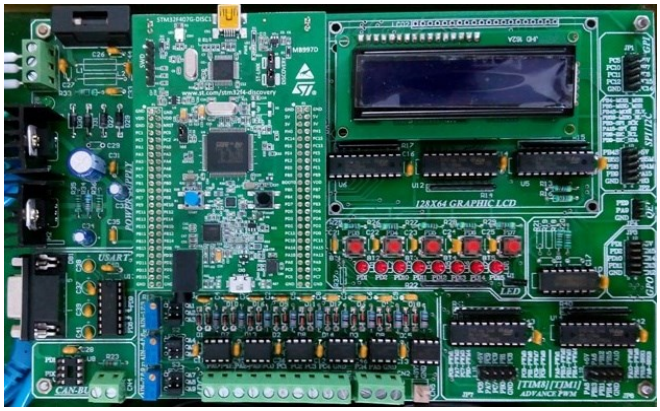

Fig. 5. Photograph of STM32F407VG Waijung compatible kit.

For generating gate pulses of CHB five-level inverter, Timer 1 and Timer 8 are utilised. The details of the timer, it's port pins, generated gate pulse (as per Fig. 2) and printed connector number on the kit is given under Table-II. The waijung block sets and software development part are discussed in further sub-section.

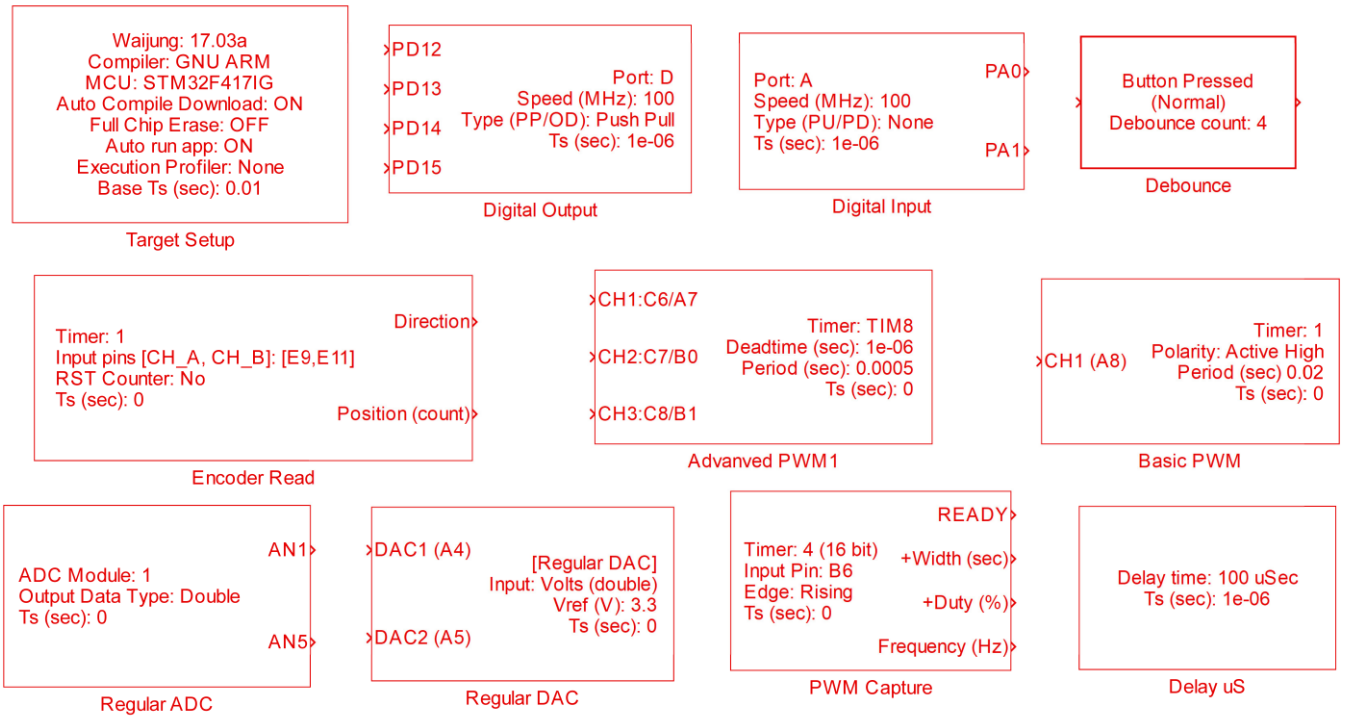


Fig. 6. Picture of Waijung Blockset Library for STM32F4 Target.

TABLE II
DETAILS OF TIMES, PORT PIN AND CONNECTOR USED FOR GATE PULSE GENERATION

| Sr.No. | Timer | Port Pins | Gate Pulse | Connector |
|---|---|---|---|---|
| 1 | 1 | PA8 | g1 | JP6 |
| | | PB13 | g2 | |
| | | PE11 | g4 | |
| | | PB14 | g3 | |
| | | PA10 | g5 | |
| | | PB15 | g6 | |
| 2 | 8 | PC6 | g8 | JP7 |
| | | PA7 | g7 | |

### A. *Programing using WAIJUNG Blockset*

For generating gate pulses MATLAB/Simulink environment with "Waijung" Blockset is explored [17]. Waijung provides Simulink Blockset to automatically generate C code from the MATLAB/Simulink simulation models. Currently, Waijung has been specifically designed to support the STM32F4 and STM32F0 targets of STMicroelectronics.

Waijung Blockset and STM32F4 target have been designed for rapid development of real-world applications with ease of use philosophy. A window containing standard Waijung Blocksets for STM32F4 Target is illustrated in Fig. 6. These Blocksets enables to perform following tasks:

- Control circuits with digital outputs and PWM outputs.
- Acquire analog and digital inputs.
- Communicate and program STM32F4 Target with USB cable.
- Inter Integrated Circuit (I2C) or Serial Peripheral Interface (SPI) protocol for peripheral devices and sensors interface.

The development of level shifted SPWM gate pulses using this environment is elaborated in next sub section.

### B. *Software Description*

Timer 1 and Timer 8 are used as time-base for generating four high frequency triangular carrier waveforms. Timers are configured using Advanced PWM block of Waijung configuring 1 kHz switching frequency. For generating gate pulses, comparison of modulating sine wave with carrier waveform is required. Sine wave magnitude is scaled in the range of 0 to 100 and used as duty ratio for generating SPWM pulses. The internal timer generates carrier wave, which is compared with the external magnitude as duty cycle and generates PWM pulses.

For level shifted SPWM comparison shown in Fig. 2, input modulating sine signal is divided into four parts for comparison with four modulating signals. The magnitude of each sinewave part is scaled, so that required comparison is done with internal carrier wave and pulses are generated. All eight gate pulses for five-level CHB inverter is generated by comparing calculated reference signals with carrier waves. The Simulink block diagram of control circuit implementation is as shown in Fig. 7.

The control logic uses frequency as an input variable. According to required frequency, the modulating sinewave magnitude is calculated, keeping *V/f* ratio constant. This modulating sinewave is processed with the aforementioned logic before connecting it to timer terminals. With the generated pulses the five-level CHB inverter is tested for variable voltage variable frequency output voltage.

### C. *Results and Discussion*

The five-level CHB inverter is tested for producing variable voltage variable frequency output. Both H-Bridges are supplied with a constant DC voltage of 30 V. At the output of the inverter, a fractional horse power, 50 Hz, 4 pole single phase induction motor is connected. User enters reference frequency and the control logic generates required level-shifted SPWM pulses to keep the *V/f* ratio constant.

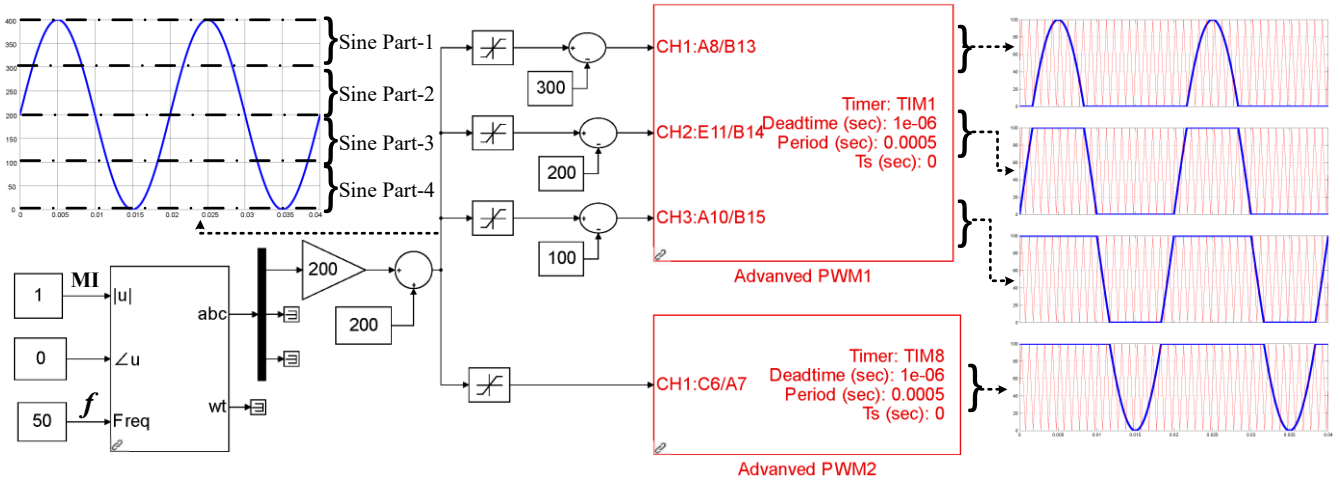


Fig. 7. Simulink Model for the Generation of Gate Pulses.

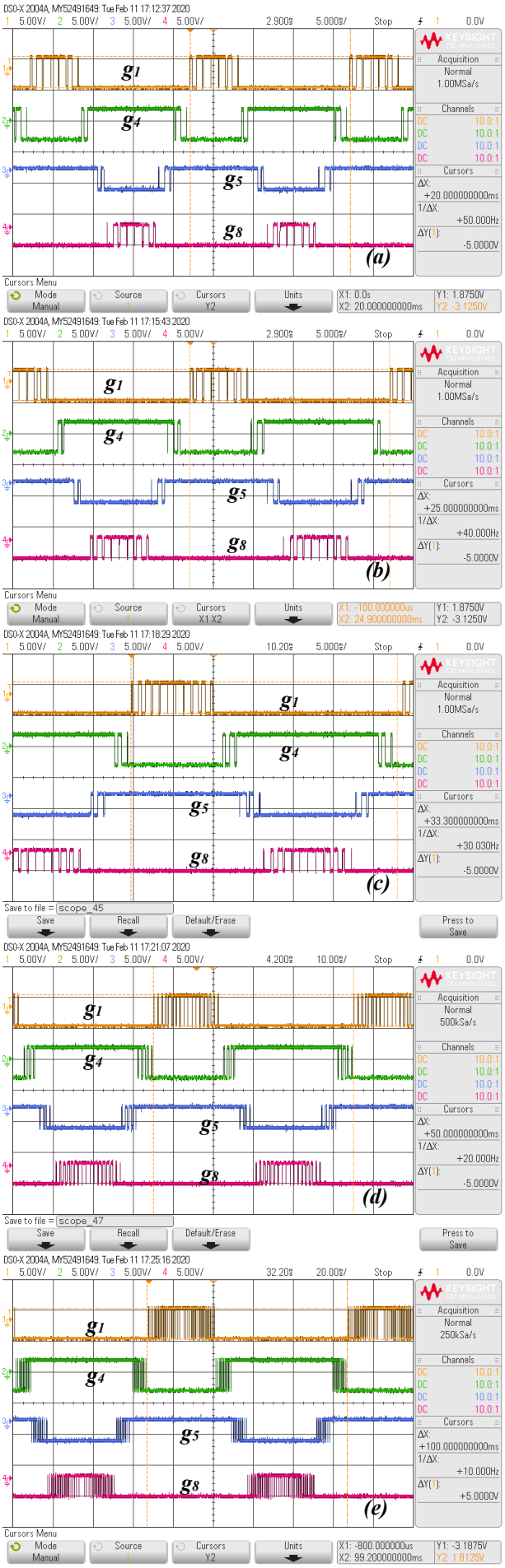


Fig. 8. Gate pulses of CHB inverter at different frequencies: (a) 50 Hz, (b) 40 Hz, (c) 30 Hz, (d) 20 Hz, and (e) 10 Hz.

The first step in experimentation is to faithfully produce the required gate pulses at different fundamental frequencies. The microcontroller is programmed using the control logic presented in Fig. 7. The oscilloscope view of gate pulses generated for different frequencies i.e. 50 Hz, 40 Hz, 30 Hz, 20 Hz and 10 Hz are as shown in Fig. 8. These gate pulses are closely in line with theoretical waveforms of Fig. 2 and it is faithfully produced by suggested model based programming. The complex logic of level shifted SPWM is easily and accurately implemented using timers.

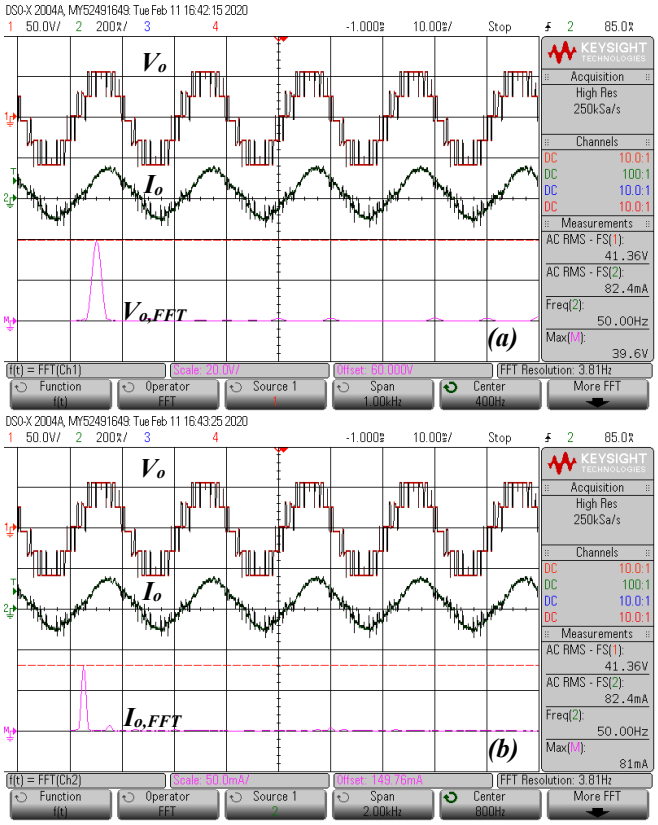


Fig. 9. Output voltage and current of the CHB inverter at 50 Hz frequency with (a) output voltage FFT, and (b) with output current FFT.

The experimental results of inverter output voltage and output current while operating CHB inverter at 50 Hz frequency is as shown in Fig. 9. Five level output voltage with applied level shifted SPWM is observed in the inverter output voltage. The lower order harmonics are absent in the inverter output voltage. Despite of low switching frequency of 1 kHz, the stator current is filtered by stator inductance and shaped approximately sinusoidal. The current waveform is observed by connecting current transformer in series with motor supply. Fig. 9(b) shows the FFT of the output current which reflects the nearly sinusoidal nature of the output current required for motor operation.

In order to vary the motor speed, it is required to vary the inverter output frequency. With a change in frequency, the RMS value of fundamental output voltage also needs to readjust simultaneously to maintain *V/f* ratio constant. This is achieved by changing frequency reference and modulation index simultaneously. Experiments were performed further at different reference frequencies and performance of the inverter is analysed further.

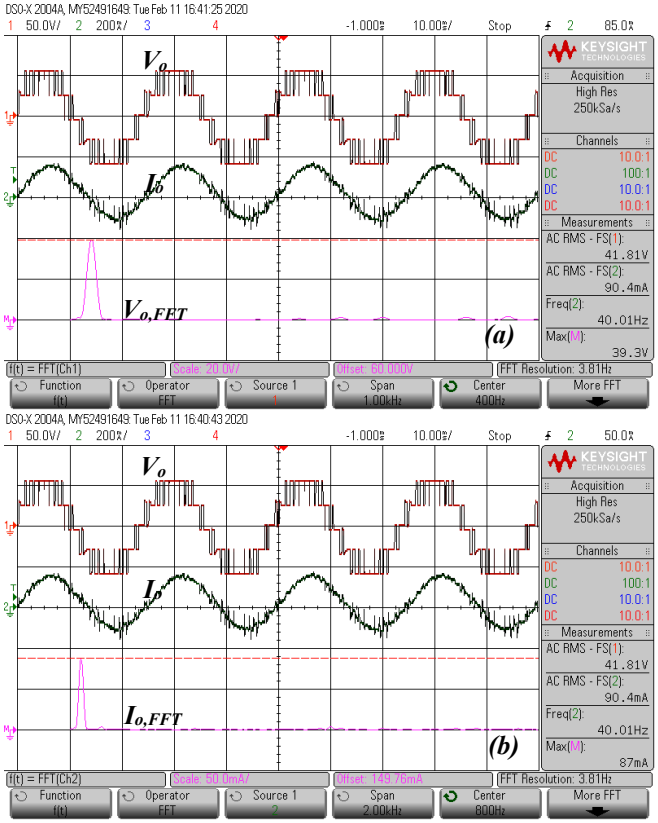


Fig. 10. Output voltage and current of the CHB inverter at 40 Hz frequency with (a) output voltage FFT, and (b) with output current FFT.

Figure 10 shows the oscilloscope view of the output voltage and output current along with their FFT, while operating the designed CHB inverter at 40 Hz frequency.

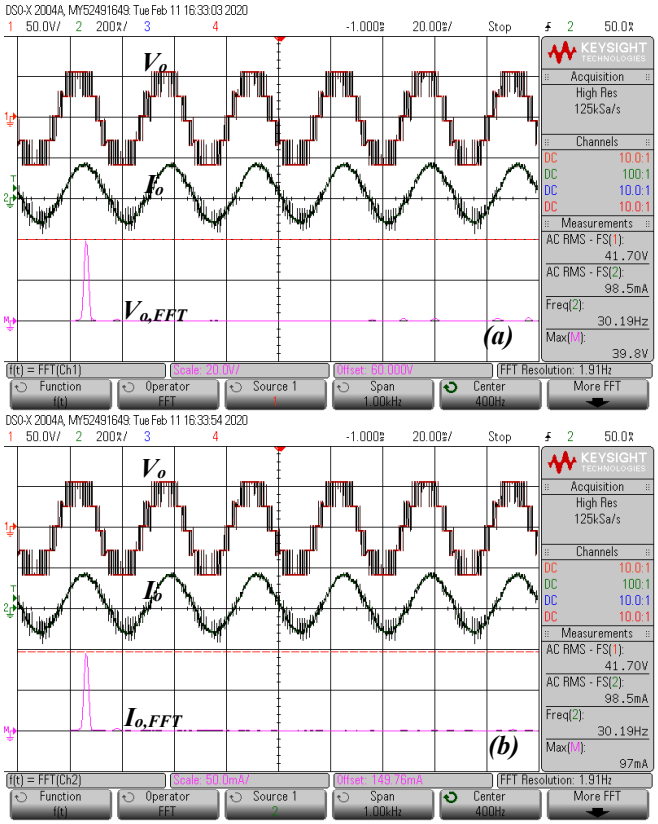


Fig. 11. Output voltage and current of the CHB inverter at 30 Hz frequency with (a) output voltage FFT, and (b) with output current FFT.

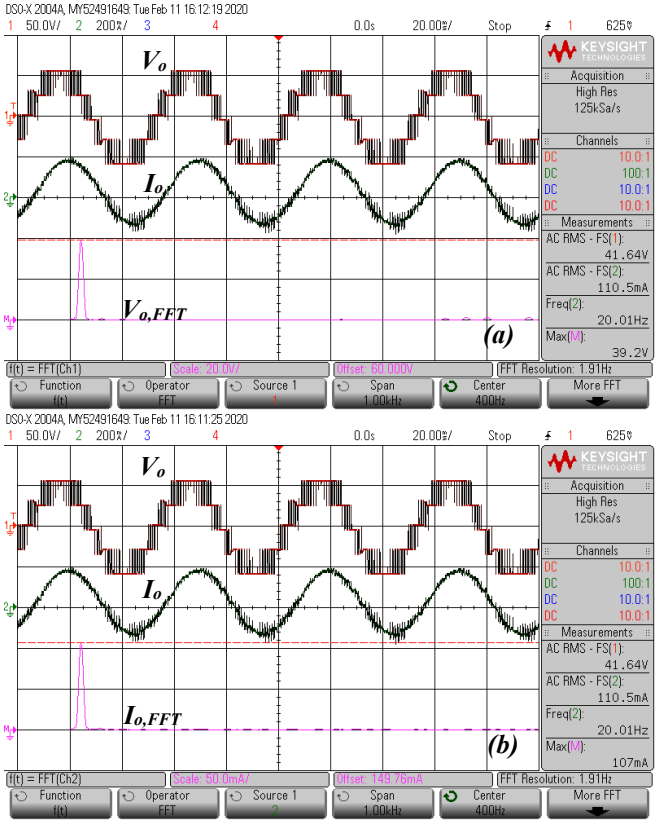


Fig. 12. Output voltage and current of the CHB inverter at 20 Hz frequency with (a) output voltage FFT, and (b) with output current FFT.

The performance of CHB inverter while operating the motor at reference set frequency of 30 Hz, 20 Hz and 10 Hz are presented in Fig. 11, 12 and 13 respectively.

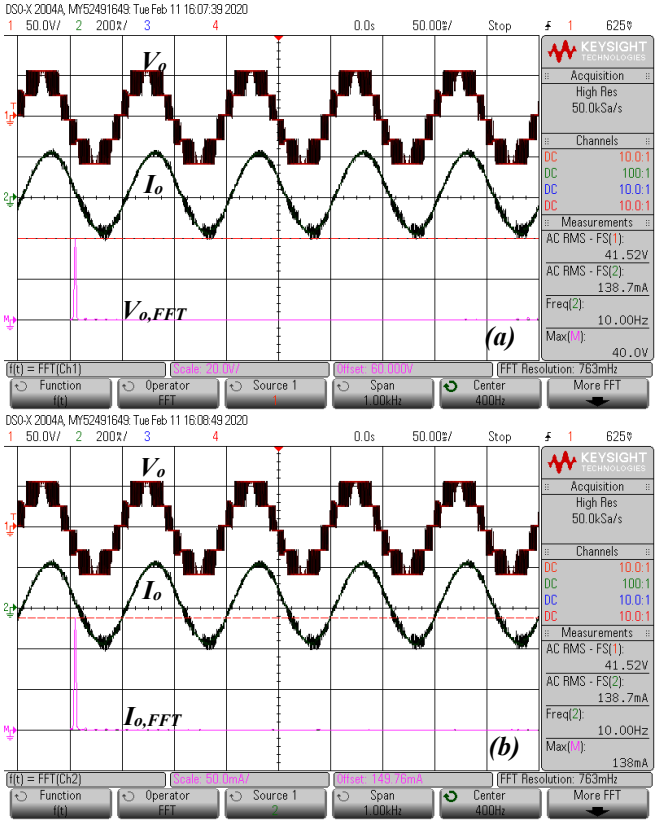


Fig. 13. Output voltage and current of the CHB inverter at 10 Hz frequency with (a) output voltage FFT, and (b) with output current FFT.

These results demonstrate that working at wide operating frequency range, the designed five-level CHB inverter produces required levels. In all the cases of testing the controller faithfully process the complex control logic of level shifted SPWM and correspondingly the motor draws nearly sinusoidal current which is required for its operation.

The magnitude of overall RMS output voltage, fundamental RMS output voltage and magnitude of different levels ($V_2$, $V_1$, $V_{-1}$, $V_{-2}$) are also observed. These values are as tabulated in Table III, while operating the inverter at three different frequencies i.e. 50 Hz, 40 Hz, and 30 Hz. It is observed from these results that working at different frequencies the developed control maintain *V/f* ratio at stator terminal constant.

TABLE III
OBSERVATIONS AT DIFFERENT FREQUENCY OPERATIONS.
DC Link Voltage E = 30 V

| Sr. No | Set *f* | $V_{rms}$ | $V_{1rms}$ | Level $V_2$ | Level $V_1$ | Level $V_{-1}$ | Level $V_{-2}$ | $V_{p-p}$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 50 | 34.80 | 31.04 | 50.50 | 24.25 | 26.25 | 52.75 | 103.75 |
| 2 | 40 | 29.70 | 26.67 | 58.50 | 29.00 | 28.00 | 58.00 | 116.50 |
| 3 | 30 | 19.64 | 17.94 | 58.00 | 27.50 | 28.00 | 57.50 | 115.50 |

The results presented by waveforms and FFT of Fig. 9 to Fig. 13 and corresponding readings of Table III shows that the inverter faithfully produces all levels and work as a variable voltage variable frequency source, which is required for controlling the speed of the induction motor. These experimental results have good accordance with the theory of level shifted SPWM controlled CHB inverter.

In summary, this work is an attempt to demonstrates an easy implementation of five-level CHB inverter implemented for the speed control of induction motor using generic ARM Cortex M4 microcontroller. Easy implementation of complex control logic of level shifted SPWM is demonstrated. Large numbers of gate pulses are generated easily using model based implementation of control logic. With the generated gate pulses the variable speed operation of the motor was observed satisfactory over a wide frequency range.

## II. CONCLUSION

In this paper, a new low cost, generic microcontroller platform for implementation of control logic of five-level CHB inverter is discussed. Programing of generic ARM core 32-bit microcontroller from MATLAB/Simulink environment is demonstrated. A close link between the simulation study and its hardware migration is realized. With the developed control five-level CHB inverter fed induction motor drive is successfully implemented. Easy implementation of large number of gate pulses using blockset based approach should encourage researchers to use multilevel inverter in place of classical two-level inverter.

## REFERENCES


[1] J. Rodriguez, J.S Lai, and F. Z Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, pp. 724-738, 2002.

[2] J.S Lai and F. Z. Peng, "Multilevel converters –A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, pp. 1098-1107, May/June 1996.

[3] Yuen-Haw Chang, and Yu-Ming Lu, "A Simple Greinacher-Doubler-Based Switched-Coupled-Inductor Boost DC-AC Inverter," Lecture Notes in Engineering and Computer Science: Proceedings of The International MultiConference of Engineers and Computer Scientists 2019, 13-15 March, 2019, Hong Kong, pp 279-284.

[4] Yuen-Haw Chang, and Kai-Lin Hsu, "A Closed-Loop Coupled-Inductor Cockcroft-Walton-Switched-Capacitor Inverter for Boost DC-AC Conversion," Lecture Notes in Eng. and Computer Science: Proceedings of The International MultiConference of Engineers and Computer Scientists, 14-16 March, 2018, Hong Kong, pp 675-680.

[5] Yuen-Haw Chang, and Zheng-Bin Li, "A High-Gain Serial-Parallel-Switched-Capacitor Coupled-Inductor Boost DC-AC Inverter," Lecture Notes in Engineering and Computer Science: Proceedings of The International MultiConference of Engineers and Computer Scientists 2017, 15-17 March, 2017, Hong Kong, pp 688-693.

[6] Jagdish Kumar, Biswarup Das, and Pramod Agarwal, "Optimized Switching Scheme of a Cascade Multilevel Inverter," Electric Power Component and Systems, vol. 38, issue 4, pp. 445-464, January 2010.

[7] G. Murali Krishna, et al. "Real-Time Implementation of a Novel Asymmetrical Multilevel Inverter with Reduced Number of Switches," Lecture Notes in Engg. and Computer Science: Proceedings of The International MultiConference of Engineers and Computer Scientists, 14-16 March 2018, Hong Kong, pp 619-623.

[8] C.T. Ma, "Investigation on Integrated Control Strategies for Grid-tied Inverters under Unbalanced Grid Voltage," Lecture Notes in Engineering and Computer Science: Proceedings of The International MultiConference of Engineers and Computer Scientists, 14-16 March, 2018, Hong Kong, pp 635-640.

[9] Cheng-Yu Yu, Gary W. Chang, Yu-Jen Liu, Raymond Y. Chang, and Yee-Der Lee, "A Study of Modelling and Inverter Controls for AC Microgrid Simulation," Lecture Notes in Engineering and Computer Science: Proceedings of The World Congress on Engineering 2017, 5-7 July, 2017, London, U.K., pp 271-276.

[10] J.Rodriguez, J.S Lai, and F. Z Peng, "Multilevel inverters : a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, pp 724-738, 2002.

[11] J.S Lai and F. Z. Peng, "Multilevel converters –A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, pp 1098-1107, May/June 1996.

[12] Reddy Sudharshana K. et al."Simulation and Experimental Validation of Common Mode Voltage in Induction Motor driven by Inverter using Arduino Microcontroller," Lecture Notes in Engineering and Computer Science: Proceedings of The World Congress on Engineering 2017, 5-7 July, 2017, London, U.K., pp 295-300.

[13] Anthony U. Adoghe et al. "Digital Speed Control of DC Motor for Industrial Automation using Pulse Width Modulation Technique," Lecture Notes in Engg. and Computer Science: Proceedings of The World Congress on Engg., 5-7 July, 2017, London, U.K., pp 371-375.

[14] Reddy Sudharshana K. et al. "Simulation with Experimental Measurement of Voltage Total Harmonic Distortion and Harmonic Frequency in Three-Phase Induction Motor fed from Inverter," Lecture Notes in Eng. and Computer Science: Proceedings of The World Congress on Engg., 5-7 July 2017, London, U.K., pp 317-322.

[15] Herman I. Verinaz Jadan et al."Deployment of a Competition Sprinter Robot over FPGA Platform with Feedback Control Systems for Velocity and Position," Lecture Notes in Eng. and Computer Science: Proceedings of The International MultiConference of Engineers and Computer Scientists, 15-17 March, 2017, Hong Kong, pp 660-665.

[16] Rodríguez, J. et al. "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Transactions on industrial electronics, 54(6), pp. 2930-2945, 2007.

[17] Waijung Blockset http://waijung.aimagin.com/