The Phase Locking Technique for Demodulators of the Binary Phase-Shift Keyed Signals

Oleg V. Chernoyarov, Vladimir P. Litvinenko, Yuliya V. Litvinenko, Boris V. Matveev, and Alexander A. Makarov

***Abstract*—We consider the fast digital algorithm for the phase locking of the coherent demodulators of the binary phase-shift keyed signals, the one similar to the well-established Costas circuit. Unlike the common counterparts, the specified algorithm can be practically implemented with the minimum number of simple arithmetic operations and it is fully compatible with the modern hardware components available. We obtain the set of nonlinear equations describing the process of phase locking and allowing us to determine the properties of the introduced digital locking algorithm analytically. By simulations, the interference immunity of the algorithm for the phase locking is demonstrated, and its operability corroborated. The possibility of its hardware implementation on the basis of the modern programmable logic devices is shown.**

***Index Terms*—Coherent demodulator, phase-shift keying, phase locking, quantization, digital signal processing**

I. Introduction

Phase locking of the reference generator of the receiver (demodulator) during the coherent radio signals processing is one of the important tasks in the design of binary phase-shift keyed (PSK) signal communication systems [1]-[4]. This problem is studied in a number of papers. Thus, various analogue and digital phase-locked systems are considered in [5]-[11]. Digital phase locking methods are of particular interest for those who develop modern digital PSK signal demodulators. The common devices [3]-[8] are intended for the direct digital representation of the analogue methods and that results in the constant need of the equipment redesign, with the expensive high-speed computing facilities required. Further we consider the fast digital algorithm for the phase locking that can be implemented with the minimum number of the simple arithmetic operations conducted within the input signal period. It allows the direct processing of the high-frequency signals to be performed at the output of the receiver intermediate-frequency section, for example.

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II. Phase Locking Methods

As it is known, the digital demodulator (Fig. 1a) transforms the input signal $s(t)$ into the sequence of discrete samples s_n by means of the analog-to-digital converter (ADC). Further, these samples are passed to the digital computing unit (DCU), which forms received information symbols S_I at its output. The samples are generated in line with the clock pulses (CPs) from the output of the clock generator (CG) operated by the synchronizing system (SS).

The SS function for coherent demodulators is to ensure the in-phase CPs position relative to the input binary PSK signal [4]-[6] as, for example, it is shown in Fig. 1b. Here CPs are marked by points, while T_0 stands for the carrier cycle.

According to [1], [12], [13], the phase-locked system should provide synchronous mode for the clock generator and the input signal, with a relative root-mean-square error no greater than several percents. The shaping of the clock signal that is synchronous with the input binary PSK signal

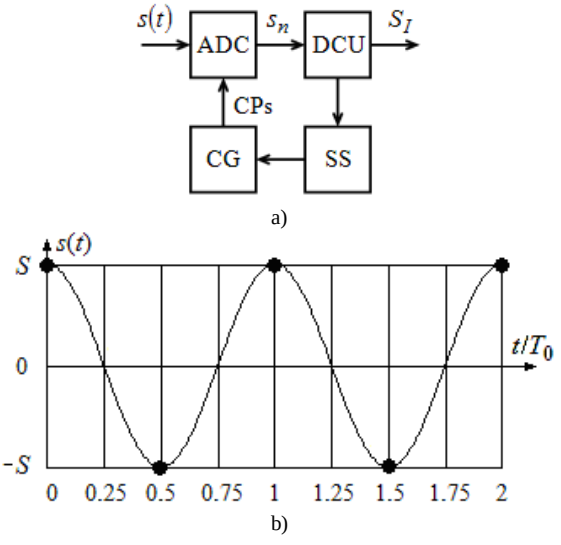

Fig. 1. The demodulator block diagram (a) and timing chart of the binary PSK signal quantization (b).

can be realized by the Pistolkors circuit [4]-[8], where frequency doubling of the input signal is implemented with the subsequent filtration and reverse frequency division. The Costas phase locking circuit shown in Fig. 2 is also widely used [6]-[9], because it does not require frequency multiplication and division in this case.

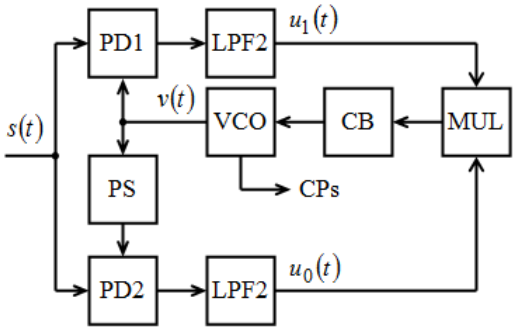

Fig. 2. The Costas circuit.

With the Costas circuit having been applied, the input PSK signal of the form

$$s(t) = S\cos(2\pi f_0 t + \psi_0) \tag{1}$$

is passed to the inputs of the phase detectors PD1 and PD2. The signal (1) initial phase is either $\psi_0 = 0$, or $\psi_0 = \pi$, and in PD1 it is compared with the phase ψ_1 of the voltage-controlled oscillator (VCO) signal

$$\nu(t) = S_1\cos(2\pi f_0 t + \psi_1),$$

while in PD2 it is compared with the phase of the signal $\nu(t)$ having passed the phase shifter (PS) by $\pi/2$.

As a result, at the outputs of the low-pass filters, namely – LPF1 and LPF2, there are formed the voltages $u_0(t)$ and $u_1(t)$ that are proportional to the values $\sin(\psi_1 - \psi_0)$ and $\cos(\psi_1 - \psi_0)$, respectively. They are passed to the multiplier (MUL) which generates the signal proportional to the value $\sin[2(\psi_1 - \psi_0)]$ and is insensitive to the input signal phase modulation. Through the control block (CB), this signal controls the VCO voltage, ensuring its phase synchronism with the input signal.

III. Fast Digital Algorithm for the Binary PSK Signals Phase Locking

The DCU speed is basically determined by the number of the required operations carried out by the digital computing unit per unit time. For the minimization of this number, the fast digital algorithm of the coherent PSK signal demodulation [14] can be used. Application of this algorithm makes it possible to design a fast digital algorithm for the phase locking, its block diagram is shown in Fig. 3.

The input binary PSK signal (1) is sampled by the ADC with the frequency $f_s = 4f_0$, forming 4 samples in synchronous mode during the period $T_0 = 1/f_0$, as it is

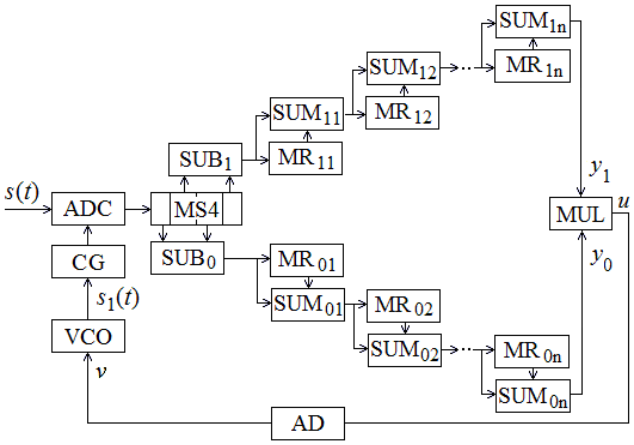

Fig. 3. The block diagram of the fast digital algorithm for the phase locking of the binary PSK signal.

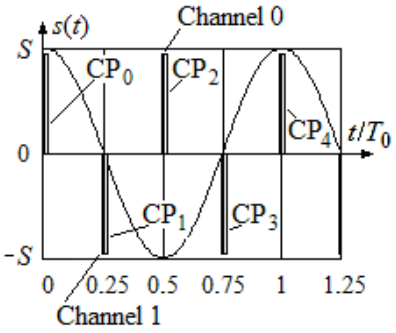

Fig. 4. Time signal diagrams.

shown in Fig. 4. The information symbol duration is equal to NT_0, where N is a number of the signal periods. Within i-th period, the clock pulses CP_{4i}, CP_{4i+1}, CP_{4i+2}, CP_{4i+3} are generated by the clock generator CG. In turn, the ADC forms the signal samples s_{4i}, s_{4i+1}, s_{4i+2}, s_{4i+3} which are saved in the multibit four-cell MS4 shifter.

The even samples s_{4i} and s_{4i+2} within the current i-th period are passed to the subtractor SUB_0. Then, in the summator SUM_{01}, the value $s_{4i} - s_{4i+2}$ is summed up with the similar value $s_{4(i-1)} - s_{4(i-1)+2}$ for the previous period which has been memorized in the multibit single-cell MR_{01} shifter earlier. And after that, the value $s_{4(i-1)} - s_{4(i-1)+2}$ is rewritten by the new value $s_{4i} - s_{4i+2}$. By the summator SUM_{02}, the value $s_{i,2} = (s_{4i} - s_{4i+2}) + (s_{4(i-1)} - s_{4(i-1)+2})$ obtained in SUM_{01} is summed up with the sum $s_{(i-2),2} = (s_{4(i-3)} - s_{4(i-3)+2}) + (s_{4(i-2)} - s_{4(i-2)+2})$ calculated for the $(i-2)$-th period and previously memorized in the multibit three-cell MR_{02} shifter. The value $s_{i,2}$ is entered into the first MR_{02} cell shifting the previously saved numbers and, as a result, the value $s_{(i-2),2}$ is pushed out from the shifter. Further the similar calculations are performed, producing the value $y_{i,0}$ at the summator SUM_{0n} output and under $i \geq N-1$, that is in fact the sum of $s_{4(i-j)} - s_{4(i-j)+2}$ differences for the i-th and $(N-1)$

number of the preceding periods of the received signal:

$$y_{i,0} = \sum_{j=0}^{N-1} \left(s_{4(i-j)} - s_{4(i-j)+2} \right). \quad (2)$$

For $i < N-1$, the transient process of the shifters zerofilling occurs (the samples with negative indexes are considered as equal to zero).

The number n of the MR-SUM operating steps is equal to $n = \log_2 N$, and the number of the periods T_0 within the information symbol is $N = 2^n$, respectively. For example, if $N = 1024$, then $n = 10$ steps are required only to calculate the sum (2). This allows us to name such algorithm the fast one.

In the same way the odd samples s_{4i+1} and s_{4i+3} are processed in SUB_1, SUM_{01}, and so on. As a result, the value

$$y_{i,1} = \sum_{j=0}^{N-1} \left(s_{4(i-j)+1} - s_{4(i-j)+3} \right) \quad (3)$$

is formed at the summator SUM_{1n} output. Thus, processing of even and odd signal samples is conducted through the two quadrature channels – y_0 and y_1, accordingly. Their responses are passed to the multiplier MUL. The obtained products $u_i = y_{i,0} y_{i,1}$ are transmitted to the averaging device (AD) forming the control action v for the VCO. The reference signal $s_1(t)$ from the VCO determines the CG pulses time position.

The considered fast digital algorithm for the phase locking is similar to the algorithm of the Costas circuit operation [6]-[9] described above, but it is transformed for the digital implementation providing the minimum number of the simple arithmetic operations over a signal period. The input signal digitization by 4 samples within the period with the further processing of even and odd samples in the multibit shifter MS4 and subtractors SUB_1 and SUB_2 realizes the phase detection of the received and the clock signals in the quadrature channels. The subsequent accumulation of the samples in the branches of the fast signal processing algorithm provides a low-frequency filtration of the samples, and then the operations are carried out, in accordance with the Costas circuit, with the subsequent transformation of the harmonious VCO voltage into the clock CG pulses.

Generally the quantization pulses from CG are shifted temporarily by the value

$$\Delta t = -\varphi / 2\pi f_0$$

where $\varphi = \psi_1 - \psi_2$ is the phase shifting between the received signal $s(t)$ and the VCO signal $s_1(t)$ by which the clock pulses are formed.

It should be noted that the digital implementation of the considered processing algorithm provides the stability of the synchronization device in a changing operating environment.

IV. The Time Diagrams

The time diagrams for the normalized quadrature channels responses

$$\tilde{y}_{i,0} = y_{i,0} / NS, \qquad \tilde{y}_{i,1} = y_{i,1} / NS \quad (4)$$

obtained by simulation in case of coherent binary PSK signal demodulation in synchronous but out-of-phase mode are shown in Fig. 5. Therein $\varphi = 0.5$ and interferences are absent. The solid line corresponds to $\tilde{y}_{i,0}$, the dashed line – to $\tilde{y}_{i,1}$, and here and throughout i is the number of the current period (counted from the start of the demodulator operation). The integer values of i/N signify the information signals ends. We can see that both responses of the quadrature channels are present here and that if $\varphi = 0$, then $y_{i,1} = 0$, and if $\varphi = \pm\pi$, then $y_{i,0} = 0$, respectively. Within the interval $0 \le i/N < 1$ the transient process occurs of the multibit shifters filling.

It is easy to show that the normalized multiplier response within one information symbol is equal to

$$u'_j = u_j / (2NS)^2 = \begin{cases} -0.5\sin(2\varphi), & \text{if } \Delta\varphi = 0, \\ -0.5(1 - 2j/N)^2 \sin(2\varphi), & \text{if } \Delta\varphi = \pm\pi. \end{cases} \quad (5)$$

Here j is the number of the current period from the beginning of the symbol being received ($j = \overline{0, N-1}$); $\Delta\varphi = 0$, if the phases of the symbol being received and the previous symbol coincide, and $\Delta\varphi = \pm\pi$, if they are opposite. When the sign of φ changes, then the sign of the product $y_{j,0} y_{j,1} / (2NS)^2$ changes too, and under $\varphi = 0$ (or $\varphi = \pi$) this product and the value v (see Fig. 3) are equal to zero.

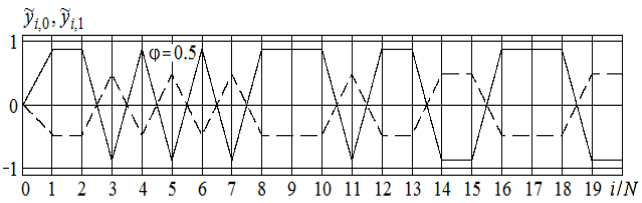

Fig. 5. The time diagrams of the quadrature channels responses.

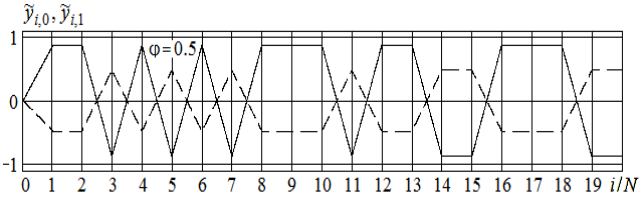

Fig. 6. The time diagrams of the multiplier response.

The time diagrams for the signal u_i' obtained through the simulation are shown at the multiplier output for the random symbol stream in Fig. 6. The parabolic form of the pulses occurring when the symbol phase is changing corresponds to (5).

According to (5), the mean value u_{mean} of the normalized multiplier response for the equiprobable information symbols is equal to

$$u_{\text{mean}} = -\frac{1}{4}\sin(2\varphi)\left[1+\frac{1}{N}\sum_{j=0}^{N-1}\left(1-\frac{2j}{N}\right)^2\right] = \\ = -\frac{1}{4}\sin(2\varphi)\left(1+\frac{1}{3}+\frac{2}{3N^2}\right) \approx -\frac{1}{3}\sin(2\varphi). \quad (6)$$

We can see that the values u_i (without averaging) or $v = u_{\text{mean}}$ (if there is averaging) operating the VCO frequency are proportional to the phase shift between the received and the reference signals, when $|\varphi| < \pi/4$. The values u_i change in time (Fig. 6), and for their quantities averaged in the AD (Fig. 3) there take place the smoothed oscillations, the ones tending to u_{mean} with the increase of the averaging interval.

V. The Combined Equations

Let us consider the locker operation from the point of time *t*. For the subsequent quantization points t_{ik} with the sampling period $T = T_0/4$ and the sampling rate (VCO frequency) $f = 1/T$ (supposed invariable during *N* periods), at the *i*-th period and the *k*-th cycle, we write down:

$$t_{ik} = T(i + k/4) - \Delta = (i + k/4)/f - \Delta. \quad (7)$$

Here $k = 0,1,2,3$, while forming 4 samples per period, and Δ is the bias of the quantization points from the synchronous mode (Fig. 4) under $f = f_0$. The example of time diagrams is shown in Fig. 7.

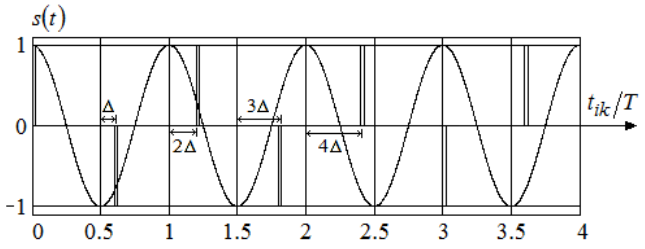

Fig. 7. The time quantization diagram.

From (7) we get

$$t_{ik} = T(i + k/4) - (1/f_0 - 1/f)(i + k/4) - \Delta = t_{ik}^* - \Delta t_{eik},$$

where $t_{ik}^* = T(i + k/4)$ are the quantization points in the synchronous mode,

$$\Delta t_{eik} = (1/f_0 - 1/f)(i + k/4) + \Delta = \\ = (i + k/4)(f - f_0)/f_0 f + \Delta = (i + k/4)\Delta f / f_0 f + \Delta \quad (8)$$

is the equivalent bias of the quantization points within the *i*-th period relative to the synchronous mode; $\Delta f = f - f_0$ is the bias of the VCO frequency relative to the signal carrier frequency. From Eq. (8) it follows that, under low detuning, namely, when $\Delta f = f - f_0 << f_0$, the bias is equal to $\Delta t_{eik} \approx T(Tf - 1)(i + k/4) + \Delta$.

We presuppose that the equivalent bias Δt_{eik} changes little over the signal period, so $\Delta t_{eik} = \Delta t_{ei0}$. Then

$$\Delta t_{ei0} = \Delta t_{ei} = \Delta f T^2 i + \Delta = T(Tf - 1)i + \Delta. \quad (9)$$

We designate the value equal to the bias of the VCO clock signals over single period as $\Delta_0 = T(Tf - 1)$ and rewrite the expression (9) into $\Delta t_{ei} = \Delta_0 i + \Delta$.

The control responses u_i or $v_i = u_{\text{mean}}$ change the VCO frequency *f* so that the value Δt_{ei} tends to zero and *f* – to f_0. The current phase shift φ_i between the signal being received and the reference signal is equal to

$$\varphi_i = -2\pi f \Delta t_{ei} \approx -2\pi f \left[T(fT - 1)i + \Delta \right].$$

The responses of the quadrature channels y_{0i} (2) and y_{1i} (3) under the constant signal amplitude *S* and the slowly varying phase shift φ_i (it is in fact invariable during the signal period) can be approximately written down for $i \geq N - 1$ in the form of

$$y_{0i} = \sum_{j=0}^{N-1} 2S\cos(\varphi_{i-j}), \qquad y_{1i} = \sum_{j=0}^{N-1} 2S\sin(\varphi_{i-j}),$$

or in the form of difference equations

If $a_k = v_k = 1$ and $u = r = 1$, then the moments (8) factorize by the estimated signal parameters and allow the multiplicative representation

$$y_{0i} = y_{0i-1} + 2S\cos(\varphi_i) - 2S\cos(\varphi_{i-N}), \\ y_{1i} = y_{1i-1} + 2S\sin(\varphi_i) - 2S\sin(\varphi_{i-N}).$$

After the multiplier we obtain the following control response $u_i = y_{0i} y_{1i}$ and by accumulation during *L* periods after the averaging device we get the VCO control signal in the form of

$$v_i = \sum_{k=0}^{L-1} u_{i-k} = \sum_{k=0}^{L-1} y_{0i-k} y_{1i-k}$$

Within the relatively short range of the VCO frequency *f* variation it is possible to consider the control characteristic

as linear, that is

$$f_i = f_{0i} - \frac{Av_i}{(2NS)^2} = f_0 - \frac{A}{(2NS)^2}\sum_{k=0}^{L-1} y_{0i-k}y_{1i-k},$$

where A is the coefficient of frequency control. Thus, the fast digital algorithm for the phase locking is approximately described by the following set of nonlinear difference equations

$$\begin{cases} \varphi_i = -2\pi f_i\left[T(f_iT-1)i + \Delta t\right], \\ y_{0i} = y_{0i-1} + 2S\cos(\varphi_i) - 2S\cos(\varphi_{i-N}), \\ y_{1i} = y_{1i-1} + 2S\sin(\varphi_i) - 2S\sin(\varphi_{i-N}), \\ f_i = f_0 - \dfrac{A}{(2NS)^2}\sum_{k=0}^{L} y_{0i-k}y_{1i-k} \end{cases}$$

with the specified initial values of the variables f_1, Δ and $\varphi_i = 0$, if $i<0$; $y_{00}=0$; $y_{10}=0$. These equations require the numerical iterative methods of solution. And calculations become more complex when the influence of the interferences should be taken into account. But similar difficulties also arise while analyzing the Costas circuit [9].

The study of the introduced algorithm for the phase locking has been conducted by means of simulation when it is assumed, for example, that $f_0 = 10$ MHz, $N = 256$ and the modulating signal is equiprobable. In Fig. 8a there are shown the dependences of the control response u_i', in Fig. 8b – the dependences of the frequency shift $f_i - f_0$, and in Fig. 8c – the dependences of the phase shift φ under the initial value of the frequency shift $\Delta f = f - f_0 = -100$ Hz and the initial value of the phase shift $\varphi = 0.5$ rad, while noise is absent.

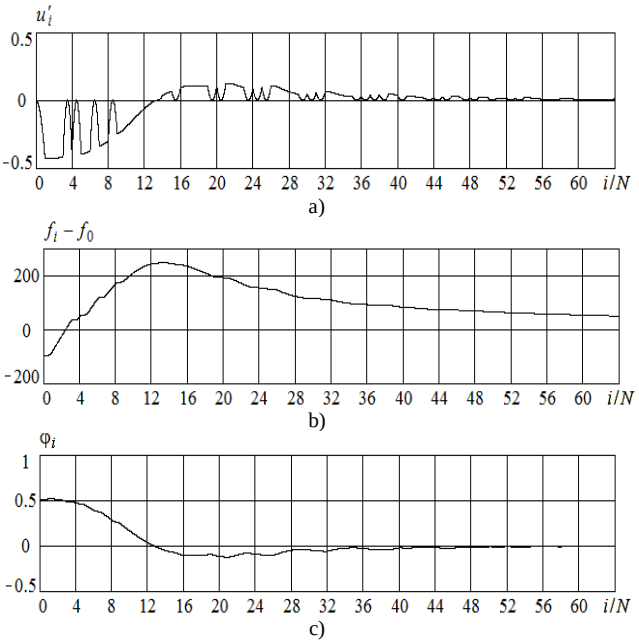

Fig. 8. The time diagrams of the control response (a), frequency shift (b) and phase shift (c) in the absence of noise.

In Fig. 9, the changes of the normalized responses of the quadrature channels (4) are given, while the phase locking is settled. It can be seen that the VCO frequency and phase approach the received signal parameters. The synchronous condition is reached after the reception of the several dozens of information symbols. And the optimal reception of PSK signal is provided in the channel corresponding to y_{0i}. When the symbol duration (number of the periods N) is decreasing, greater number of symbols is required to settle the synchronous operation.

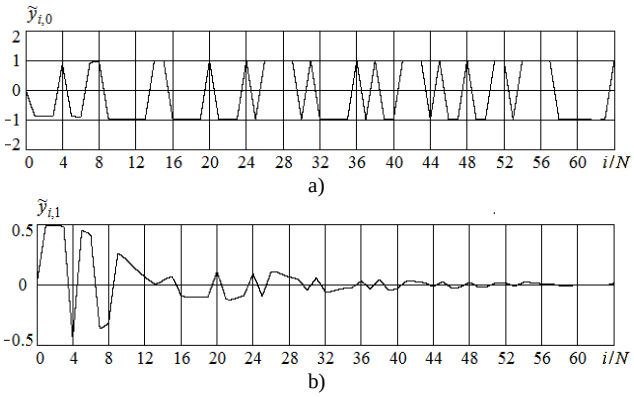

Fig. 9. Time diagrams of the normalized quadrature channel responses y_{0i} (a) and y_{1i} (b).

The influence of interferences results in fluctuations of the phase shift between the signal being received and the VCO signal. The example of simulated results under $N = 256$, $A = 0.1$, initial frequency shift $\Delta f = f - f_0 = -100$ Hz, initial phase shift $\varphi = 0.5$ rad, signal-to-noise ratio $h^2 = 12$ dB and under the influence of the stationary Gaussian noise is presented in Fig. 10.

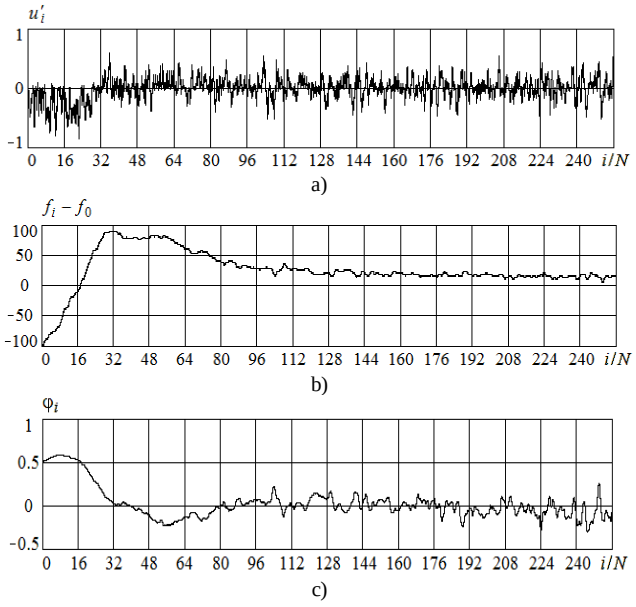

Fig. 10. Time diagrams of the control response (a), the frequency shift (b) and the phase shift (c) in the presence of noise.

In Fig. 10a, we can see the signal and noise components of the quadrature channels responses product

$u_i' = y_{0i} y_{1i} / (2NS)^2$. That leads to the smoothed oscillations of the VCO frequency (Fig. 10b) and phase (Fig. 10c) caused by the time lag of the control circuit. The root-mean-square deviation σ_φ of the oscillations of the phase shift φ is equal to $\sigma_\varphi \approx 0.1$ rad when the synchronous operation is established. It corresponds to the value that is feasible from the point of view of the demodulator interference immunity. It should be noted that the noise smoothing effect takes place (Fig.10a) in the control circuit of the VCO frequency and phase.

Fluctuations of the VCO signal phase under the influence of Gaussian interferences are determined by their strength (signal-to-noise ratio) and the time lag of the phase locking loop [5]. The following factors may cause this time lag increasing:

- increase in the number N of the periods of the signal samples accumulation in the quadrature channels;
- decrease in the coefficient A of the VCO frequency control;
- increase in the number of the signal periods during which the response of the averaging unit is formed.

In case when the signal $s(t)$ (1) is distorted by non-Gaussian interferences, due to the accumulation of the samples in summators SUM (Fig. 3) over N periods the distribution of these interferences is transformed into the Gaussian one. It follows from the central limit theorem [1], [2], in which the sum of comparable random variables with arbitrary probability densities converges to a Gaussian random value while the number of summands increases. This fact is confirmed by the results of statistical simulation.

The phase fluctuations amplify with the signal-to-noise ratio h^2 decreasing and N and A increasing. This is explained in Fig. 11 by the graphs obtained by the simulations.

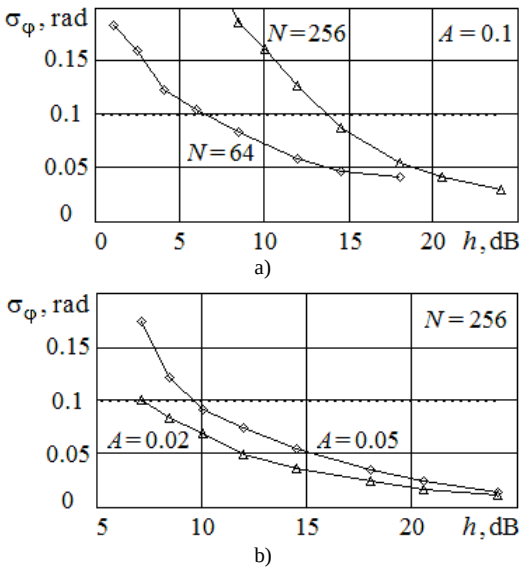

Fig. 11. The dependences of the timing error upon the signal-to-noise ratio for the fixed values of A (a) and N (b).

While averaging the VCO control response smoothes the oscillations of the phase shift φ, the transition time of the synchronous operation increases simultaneously. Under the proper conditions, the demodulator sign ambiguity occurs, which is typical for all the phase-locked systems [6]-[8]. This is so because the control signal (6) is proportional to the value of $\sin(2\varphi)$, which takes a stable value of 0 under $\varphi = 0$ and $\varphi = \pi$.

The considered locking algorithm can be implemented by means of the modern field-programmable gate arrays (FPGAs) [15]-[17], Spartan 6 or Virtex 5 among them, for example, at the signal frequencies up to 50-100 MHz.

VI. Conclusion

In order to ensure the phase locking of the coherent demodulators of the binary phase-shift keyed signals, the introduced fast digital algorithm can be applied with the minimum number of the simple arithmetic operations over a signal period. Due to the high speed, this algorithm allows immediate high-frequency signals processing, and it can be implemented on the basis of the modern programmable logic devices for 50-100 MHz.

The smoothed (rectilinear) form of the time diagrams of the responses of demodulator quadrature channels reflects the optimality of the signal samples processing procedure. Thus, in the presence of Gaussian interferences the considered locking algorithm provides the root-mean-square deviation of phase shifting fluctuations of the received and the reference signals that is not greater than 0.1 rad under the signal-to-noise ratio more than 10 dB. In addition, the samples accumulation into the quadrature channels leads to the normalization of non-Gaussian additive interferences. Thus, in many cases this algorithm can be used for the demodulation of the signals against non-Gaussian distortions.

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