Active Tunable Lossy Inductance Simulation Using Single Fully Balanced Voltage Differencing Buffered Amplifier

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Abstract—Two active configurations for simulating tunable floating and grounded lossy inductors are described. Each simulated inductor circuit contains only a single fully balanced-voltage differing buffered amplifier (FB-VDBA), one resistor, and one capacitor. The equivalent values of the simulated elements can be tuned independently through the FB-VDBA’s bias current and/or the resistor in the circuit. Non-ideal analysis of the synthetic inductors is also provided. The practical use of the proposed FB-VDBA based lossy inductance simulators is demonstrated on both a second-order RLC low-pass filter and a parallel RLC resonance circuit. PSPICE simulation results are provided to evaluate the presented theory.

Index Terms—Fully Balanced-Voltage Differencing Buffered Amplifier (FB-VDBA), RL impedance simulator, lossy inductor, inductance simulation

I. INTRODUCTION

An active simulation of lossy inductors has become a fascinating research topic for electrical engineers, circuit researchers, and scientists, since it is useful in active network synthesis, and microelectronic applications, such as active filters, LC oscillators, and impedance matching and parasitic cancellation circuitry. From the viewpoint of the advent of integrated circuit (IC) technology, the design of synthetic active inductances can be applied instead of the bulky discrete inductors in passive circuits. Accordingly, several active circuits for synthetic lossy inductance simulation have been developed earlier using various types of active elements [1]-[31]. These inductance simulators can usually be classified as floating [1]-[13] and grounded [14]-[31] configurations. It can be observed in [1]-[5], [7], [9], [11]-[13], [19], [21], [23] that the realizations are composed of more than one active components. Some of them also use three or more grounded and/or floating passive components [1]-[5], [9], [11], [19], [21], [23], [31]. Moreover, in [2]-[3], [5], [9], [12], any kind of critical element-matching and/or cancellation constraints are necessarily required. A topology without such matching requirements is considered to be a favorable feature for the desired realization. Apart from that, the methods in [6], [8], [10], [14]-[18], [20], [22], [24]-[30] utilize a single active component to simulate floating and grounded lossy inductors. However, the designs still need an excessive number of passive elements, i.e. at least three passive elements, and do not provide electronic control facility. In addition to [8], [14]-[15], [25]-[27], there are requirements for any certain component-matching or cancellation conditions.

The main objective of this work is, therefore, to introduce two tunable lossy inductance simulator circuits, which realize floating series RL impedance and grounded parallel RL impedance. The introduced lossy simulated inductors both employ only one fully balanced-voltage differencing buffered amplifier (FB-VDBA) [32]-[36] as well as a low number of passive elements, namely one resistor and one capacitor. The simulated inductor circuits are devoid of any certain component-matching or cancellation constraints. The simulated resistance and inductance elements of the circuits in both cases can be varied electronically by the transconductance gain of the FB-VDBA. The effects of the transfer error and parasitic elements of the FB-VDBA on the resulting inductor structures are also examined. The presented theory has been verified by simulation results based on CMOS TSMC 0.25-μm process parameters. A detailed comparison of the proposed inductance simulators with the previously similar solutions [1]-[31] is presented in Table I.

II. FULLY BALANCED-VOLTAGE DIFFERENCING BUFFERED AMPLIFIER (FB-VDBA)

The symbolic representation of the ideal FB-VDBA device is shown in Fig.1, which can be characterized by the following matrix equation [33]-[35].
**TABLE I**

PHYSICAL COMPARISON OF THE PROPOSED INDUCTANCE SIMULATORS WITH SOME EARLIER WORKS.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Inductor</th>
<th>Inductor type</th>
<th>No. of active element</th>
<th>No. of passive element</th>
<th>Matching requirement</th>
<th>Availability of electronic tuning</th>
<th>Supply voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>Floating</td>
<td>parallel (Fig.1b)</td>
<td>CCII = 2</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[2]</td>
<td>Floating</td>
<td>parallel (Fig.1c)</td>
<td>OA = 2, OTA = 1 R = 2, C = 1</td>
<td>yes</td>
<td>no</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>[3]</td>
<td>Floating</td>
<td>parallel (Fig.2a)</td>
<td>OA = 2</td>
<td>R = 3, C = 2</td>
<td>yes</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[4]</td>
<td>Floating</td>
<td>series, parallel (Fig.2b, 3f, 3g)</td>
<td>CCII = 2</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[5]</td>
<td>Floating</td>
<td>parallel (Fig.3a)</td>
<td>CCII = 2 R = 3, C = 2</td>
<td>yes</td>
<td>no</td>
<td>±12V</td>
<td></td>
</tr>
<tr>
<td>[6]</td>
<td>Floating</td>
<td>series, parallel (Fig.3c)</td>
<td>CCII = 1 R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>[7]</td>
<td>Floating</td>
<td>series, parallel (Fig.2)</td>
<td>CCCII = 1, CCCIII = 1</td>
<td>C = 1</td>
<td>no</td>
<td>yes</td>
<td>±2.5V (simulation), ±5V (experiment)</td>
</tr>
<tr>
<td>[8]</td>
<td>Floating</td>
<td>series/parallel (Fig.2a)</td>
<td>DDCC = 1 R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>±0.9V, -0.34V</td>
<td></td>
</tr>
<tr>
<td>[9]</td>
<td>Floating</td>
<td>parallel (Fig.2a)</td>
<td>CFOA = 2 R = 3, C = 2</td>
<td>yes</td>
<td>no</td>
<td>±15V</td>
<td></td>
</tr>
<tr>
<td>[10]</td>
<td>Floating</td>
<td>parallel (Fig.1a)</td>
<td>VDBA = 1 R = 2, C = 1</td>
<td>yes</td>
<td>yes</td>
<td>±0.75V (simulation), ±5V (experiment)</td>
<td></td>
</tr>
<tr>
<td>[11]</td>
<td>Floating</td>
<td>parallel (Fig.1b)</td>
<td>VDBA = 2 R = 1, C = 1</td>
<td>yes</td>
<td>yes</td>
<td>±1V</td>
<td></td>
</tr>
<tr>
<td>[12]</td>
<td>Floating</td>
<td>series (Fig.2a)</td>
<td>CCII = 1</td>
<td>R = 3, C = 4</td>
<td>yes</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[13]</td>
<td>Floating</td>
<td>parallel (Fig.1a)</td>
<td>CCII = 1</td>
<td>R = 3, C = 1</td>
<td>yes</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[14]</td>
<td>Floating</td>
<td>parallel (Fig.1b)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>yes</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[15]</td>
<td>Grounded</td>
<td>parallel (Fig.1e)</td>
<td>CCII = 1</td>
<td>R = 3, C = 2</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[16]</td>
<td>Grounded</td>
<td>parallel (Fig.1f)</td>
<td>CCII = 1</td>
<td>R = 3, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[17]</td>
<td>Grounded</td>
<td>parallel (Fig.2a)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[18]</td>
<td>Grounded</td>
<td>parallel (Fig.2b)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[19]</td>
<td>Grounded</td>
<td>parallel (Fig.3a)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[20]</td>
<td>Grounded</td>
<td>parallel (Fig.3b)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[21]</td>
<td>Grounded</td>
<td>parallel (Fig.3c)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[22]</td>
<td>Grounded</td>
<td>parallel (Fig.3d)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[23]</td>
<td>Grounded</td>
<td>parallel (Fig.3e)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[24]</td>
<td>Grounded</td>
<td>parallel (Fig.3f)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[25]</td>
<td>Grounded</td>
<td>parallel (Fig.3g)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[26]</td>
<td>Grounded</td>
<td>parallel (Fig.3h)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[27]</td>
<td>Grounded</td>
<td>series (Fig.3a)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[28]</td>
<td>Grounded</td>
<td>series (Fig.3b)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[29]</td>
<td>Grounded</td>
<td>series (Fig.3c)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[30]</td>
<td>Grounded</td>
<td>series (Fig.3d)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
<tr>
<td>[31]</td>
<td>Grounded</td>
<td>series (Fig.3e)</td>
<td>CCII = 1</td>
<td>R = 2, C = 1</td>
<td>no</td>
<td>no</td>
<td>NA</td>
</tr>
</tbody>
</table>

NA: Not Available


The mathematical model of the FB-VDBA in the small-signal circuit is given by

\[
\begin{bmatrix}
    i_{z1} \\
    i_{z2} \\
    v_{w+} \\
    v_{w-}
\end{bmatrix} =
\begin{bmatrix}
    -\alpha_p g_m & -\alpha_p g_m & 0 & 0 \\
    \alpha_p g_m & \alpha_p g_m & 0 & 0 \\
    0 & 0 & \beta_p & 0 \\
    0 & 0 & 0 & \beta_p
\end{bmatrix}
\begin{bmatrix}
    v_p \\
    v_w \\
    v_{w+} \\
    v_{w-}
\end{bmatrix}
\]

In (1), \( g_m \) is the small-signal transconductance gain of the FB-VDBA, which is scaled electronically by electronic means. Also, the parameters \( \alpha_p \) and \( \beta_p \) (\( i = p, n \)) are respectively the non-ideal transconductance gains and the
non-ideal voltage gains, which are equal to unity in the ideal case. The possible structure realization of the FB-VDBA is given in Fig. 2, where its internal part is functionally a connection of dual-out operational transconductance amplifier (OTA) M\textsubscript{1}-M\textsubscript{12} and two voltage buffers M\textsubscript{13}-M\textsubscript{16} and M\textsubscript{17}-M\textsubscript{20} \cite{33}-\cite{35}. Therefore, this device utilizes features of tunable OTA and voltage follower in a single integrated circuit structure. The FB-VDBA transconductance gain, which is realized in the OTA stage, is determined by the following relation.

\[ g_m = \sqrt{K I_B} \]  \hspace{1cm} (2)

where \( K = \mu C_{ox} W/L \) is the MOS transistor transconductance, \( W \) and \( L \) are the channel width and length, respectively, \( \mu \) is the carrier and \( C_{ox} \) is the gate-oxide capacitance per unit area. In this design, the transistor dimensions \((W/L)\) of the FB-VDBA realization in Fig.2 are given in Table II.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W/L ((\mu m/\mu m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>M\textsubscript{1}-M\textsubscript{2}</td>
<td>8/0.25</td>
</tr>
<tr>
<td>M\textsubscript{3}, M\textsubscript{6}</td>
<td>12/0.25</td>
</tr>
<tr>
<td>M\textsubscript{4}-M\textsubscript{5}, M\textsubscript{7}-M\textsubscript{12}</td>
<td>20/0.25</td>
</tr>
<tr>
<td>M\textsubscript{13}-M\textsubscript{20}</td>
<td>60/0.25</td>
</tr>
</tbody>
</table>

III. PROPOSED LOSSY INDUCTANCE SIMULATOR CIRCUITS

The proposed circuits for realizing floating and grounded lossy inductors are shown in Fig.3 and 4, respectively. Both of the circuits are implemented with a single FB-VDBA, one resistor, and one capacitor. For the ideal case, i.e. \( \alpha = \beta = 1 \), the input impedance and admittance functions of the proposed inductance simulators in Fig.3 and 4 are respectively obtained as follows:

\[ Z_{in1} = \frac{v_{in1}}{i_{in1}} = R_{eq1} + s L_{eq1} = \frac{1}{g_m} + \left( \frac{R C_1}{g_m} \right), \]  \hspace{1cm} (3)

and

\[ Y_{in2} = \frac{I_{in2}}{V_{in2}} = \frac{1}{R_{eq2}} + \frac{1}{s L_{eq2}} = \frac{1}{R_2} + \frac{g_m}{s R_2 C_2}. \]  \hspace{1cm} (4)

From these results, it follows that the proposed circuit of Fig.3 simulates a floating lossy series RL-type inductor with equivalent resistance \( R_{eq1} = 1/g_m \) and equivalent inductance \( L_{eq1} = R_1 C_1/g_m \), and the proposed circuit of Fig.4 realizes a grounded parallel RL impedance with \( R_{eq2} = R_2 \) and \( L_{eq2} = R_2 C_2/g_m \). It is further observed that in both circuits the simulated inductance value is adjustable independently via \( R_1 \) and/or \( C_1 \) in the circuit of Fig.3, and via \( g_m \) and/or \( C_2 \) in the circuit of Fig.4. Two proposed circuits are also free from any passive component-matching constraints for inductance simulations.

IV. EFFECT OF TRANSFER ERRORS

Considering the non-ideal parameters \( \alpha \) and \( \beta \) gave in (1), the one-point impedance function looking into terminal 1 for the simulator circuit in Fig.3 can be found as:

\[ Z_{in1} \big|_{\beta=0} = \frac{v_{in1}}{i_{in1}} = R_{eq1} + s L_{eq1} = \left( \frac{1}{\alpha_0 g_m} \right) + \left( \frac{R C_1}{g_m} \right) \left( \frac{\beta_0}{\alpha_0} \right). \]  \hspace{1cm} (5)
On the other hand, the one-point impedance function looking into terminal 2 of Fig.3 can be written as:

\[ Z_{\text{out}}^{*}|_{b1=0} = \frac{-v_{\text{in}}}{i_{\text{in}}} = R_{\text{eq1}} + sL_{\text{eq1}}^{*} = \left( \frac{1}{\alpha_{g} g_{m}} \right) + \left( \frac{R_{\text{eq1}}}{g_{m}} \right) \left( \frac{\beta_{p}}{\alpha_{p}} \right). \]  \hspace{1cm} (6)

In the same way, the \( \alpha_{g} \) and \( \beta_{p} \) gains are also taken into consideration to evaluate the performance of the second developed lossy parallel-type inductance simulator of Fig.4. Therefore, considering non-idealities into account, the input admittance from (4) modifies as:

\[ Y_{\text{in}} = \frac{i_{\text{in}}}{v_{\text{in}}} = \frac{1}{sR_{\text{eq2}}} + \frac{sL_{\text{eq}}^{*}}{R_{\text{eq2}}} = \left( \frac{g_{m} \alpha_{g} \beta_{p}}{sR_{c2} C_{2}} \right). \]  \hspace{1cm} (7)

It readily shows in (5)-(7) that the non-ideal transfer gains of FB-VDBA affect the input equivalent impedances of the proposed circuits, and as a result lesser the \( \alpha_{g} \) and \( \beta_{p} \) non-ideal gains, the lesser is the influence on the simulator. It is also noted that the proper tuning of the \( g_{m} \)-value may practically lead to the reduction of the non-ideal transfer gain effect.

V. EFFECT OF PARASITIC IMPEDANCES

Consider the non-ideal behavior model of the FB-VDBA shown in Fig.5. The shunt parasitic impedances \( (R/C) \) appear at terminals \( p, n, z^{+}, \) and \( z^{-} \), respectively, whereas the resistances \( R_{\text{eq1}} \) and \( R_{\text{eq2}} \) are the serial parasitic resistances at terminals \( w^{+} \) and \( w^{-} \). Using the non-ideal model of the FB-VDBA in presence of parasitic impedances, the proposed inductance simulator circuits in Fig.3 and 4 can be redrawn as represented in Fig.6 and 7, respectively. Thus, taking into account the FB-VDBA parasitics outlined above and reanalyzing the real behavior of the proposed floating lossy inductance simulator in Fig.6, the non-ideal input impedance becomes:

\[ Z_{\text{in}} = \left[ \frac{1}{g_{m}(1+sR_{\text{eq1}} C_{1})} \right] + \left[ \frac{s(R_{1} + R_{2} + R_{\text{eq1}})C_{1}}{g_{m}(1+sR_{\text{eq1}} C_{1})} \right]. \]  \hspace{1cm} (8)

Assumed that in practice the above relation is \( R_{1} > R_{\text{eq1}}, \) \( R_{2} > R_{\text{eq1}} \), then the impedance \( Z_{\text{in}} \) can be approximated to

\[ Z_{\text{in}} = Z_{1} + Z_{2} \approx \left[ \frac{1}{g_{m}(1+sR_{\text{eq1}} C_{1})} \right] + \left[ \frac{sR_{C1}}{g_{m}(1+sR_{\text{eq1}} C_{1})} \right], \]  \hspace{1cm} (9)

where

\[ Y_{1} = \frac{1}{Z_{1}} = \frac{g_{m} + s(g_{m} R_{\text{eq1}} C_{1})}{1}, \]  \hspace{1cm} (10)

and

\[ Y_{2} = \frac{1}{Z_{2}} = \left[ \frac{g_{m}}{sR_{C1}} \right] + \left[ \frac{g_{m} R_{\text{eq1}}}{sR_{C1} R_{1}} \right] + \frac{1}{sL_{\text{eq}}^{*}}. \]  \hspace{1cm} (11)

From (9)-(11), it is important to note that an extra intrinsic capacitance \( C_{\text{ext}} \) appears in shunt with the parasitic resistance \( R_{\text{eq1}} \). It may be also mentioned that in the same branch an extra intrinsic resistance \( R_{\text{eq1}} \) is also in parallel with the parasitic inductance \( L_{\text{eq1}}^{*} \). Thus, if the FB-VDBA parasitic impedances are included, an equivalent circuit of the proposed floating lossy inductance simulator in Fig.3 is redrawn in Fig.8. However, if the condition \( R_{\text{eq1}} << 1/g_{m} R_{1} \) is satisfied, then the parasitic effects of the FB-VDBA are reduced.

Fig. 5. Non-ideal model of the FB-VDBA with parasitic elements.

Fig. 6. Proposed floating lossy inductance simulator of Fig.3 including parasitic elements.

Fig. 7. Proposed grounded lossy inductance simulator of Fig.4 including parasitic elements.

Similarly, for the proposed grounded lossy inductor in Fig.7, the input admittance for the common case of \( C_{2} >> C_{n}, C_{z}, \) and \( R_{z} >> R_{n} \), is found approximately as:

\[ Y_{\text{in}} = Y_{A} + Y_{B} \approx \left[ \frac{sR_{C2}(1+g_{m} R_{\text{eq2}})}{(R_{2} + R_{\text{eq2}})(1+sR_{C2})} \right] + \left[ \frac{g_{m} R_{C1}}{(R_{2} + R_{\text{eq2}})(1+sR_{C2})} \right], \]  \hspace{1cm} (12)

where

\[ Z_{2} = \frac{1}{Y_{d}} = \left[ \frac{R_{2} + R_{\text{eq2}}}{1 + g_{m} R_{\text{eq2}}} \right] + \left[ \frac{R_{2} + R_{\text{eq2}}}{sR_{C1}(1+g_{m} R_{\text{eq2}})C_{2}} \right] = R_{\text{eq2}} + \frac{1}{sC_{\text{ext2}}}, \]  \hspace{1cm} (13)
\[ Z_{\text{eq}} = \frac{1}{g_m} \left[ \frac{(R_1 + R_{\text{eq}})C_2}{g_m} \right] + \left( \frac{R_1 + R_{\text{eq}}}{g_m} \right) = sL_{\text{eq}2} + R_{\text{eq}2} \] (14)

From (12)-(14), an equivalent circuit including FB-VDBA parasitic impedances for the proposed inductance simulator circuit in Fig.4 can be represented in Fig.9. One observes inductance simulator in Fig.4 including parasitic impedances.

\[ \text{vin} = 0.2 \text{mH} \]

In Fig.10, it is found that the phase shift between parasitic resistance \[ R_{\text{eq}} \] is high enough, the extra impedances \( (R_{\text{ext2}} \text{ and } C_{\text{ext2}}) \) do not affect the impedance of the inductor.

\[ \text{vin} = 0.2 \text{mH} \]

VI. SIMULATIONS AND FUNCTIONAL VERIFICATIONS

To verify the functionality of the proposed lossy inductance simulator circuits, PSPICE simulations were carried out based on a standard 0.25-\( \mu \text{m} \) CMOS process parameters from TSMC [37]. The proposed circuits in Fig.3 and 4 are simulated by using the FB-VDBA in Fig.2 with power supply voltages fixed at \( \pm 0.75 \text{ V} \).

A. Simulation results of the proposed floating lossy inductance simulator circuit in Fig.3

The simulated transient responses of the proposed circuit in Fig.3 are represented in Fig.10 with \( g_m = 0.5 \text{ mA/V} \) (\( I_B \approx 30 \mu\text{A} \)), \( R_1 = 1 \text{k}\Omega \) and \( C_1 = 0.1 \text{nF} \). Using (3), the simulated equivalent elements are obtained as \( R_{\text{eq}} = 2 \text{k}\Omega \) and \( L_{\text{eq}} = 0.2 \text{ mH} \). In Fig.10, it is found that the phase shift between \( v_{\text{in1}} \) and \( i_{\text{in1}} \) is about 31° when the sinusoidal input signal of an amplitude 80 mV (peak) at 1 MHz was applied to the circuit. On the other hand, the simulation and ideal frequency characteristics of the impedance \( Z_{\text{in1}} \) are also plotted in Fig.11. The simulated responses agree well with the theoretical results, which confirm the proper operation of the proposed circuit. In addition to simulation results, the total power consumption of the circuit in Fig.3 was found as 14.1 mW.

\[ 10\text{m} 100\text{m} 1\text{A} 10\text{mA} 1\text{mA} 100\mu\text{A} 1\mu\text{A} 0.1\mu\text{A} 0.01\mu\text{A} 0.001\mu\text{A} \]

\[ 10\text{m} 100\text{m} 1\text{A} 10\text{mA} 1\text{mA} 100\mu\text{A} 1\mu\text{A} 0.1\mu\text{A} 0.01\mu\text{A} 0.001\mu\text{A} \]

\[ 10\text{m} 100\text{m} 1\text{A} 10\text{mA} 1\text{mA} 100\mu\text{A} 1\mu\text{A} 0.1\mu\text{A} 0.01\mu\text{A} 0.001\mu\text{A} \]

\[ 10\text{m} 100\text{m} 1\text{A} 10\text{mA} 1\text{mA} 100\mu\text{A} 1\mu\text{A} 0.1\mu\text{A} 0.01\mu\text{A} 0.001\mu\text{A} \]

\[ 10\text{m} 100\text{m} 1\text{A} 10\text{mA} 1\text{mA} 100\mu\text{A} 1\mu\text{A} 0.1\mu\text{A} 0.01\mu\text{A} 0.001\mu\text{A} \]

Fig. 10. Simulated transient responses for \( v_{\text{in1}} \) and \( i_{\text{in1}} \) of the proposed floating lossy inductance simulator in Fig.3.

Fig. 11. Theoretical (dashed lines) and simulation (solid lines) magnitude and phase responses of \( Z_{\text{in1}} \) of Fig.3.

Fig.12 shows the simulated magnitude responses of \( Z_{\text{in1}} \) with \( R_{\text{eq}} \) tuning while keeping \( L_{\text{eq}} \) constant. This design is for \( L_{\text{eq}} = 0.2 \text{ mH} \) with \( C_1 = 0.1 \text{nF} \), and simultaneously changing the values of \( g_m \) and \( R_1 \) as follows: (0.25 mA/V and 0.5 kΩ), (0.50 mA/V and 1 kΩ), (0.75 mA/V and 1.5 kΩ), (1 mA/V and 2 kΩ), and (1.25 mA/V and 2.5 kΩ), which results in \( R_{\text{eq}} = 4 \text{kΩ}, 2 \text{kΩ}, 1.34 \text{kΩ}, 1 \text{kΩ}, \) and 0.8 kΩ, respectively. Fig.13 also shows the \( Z_{\text{in1}} \)-magnitude frequency variation concerning \( R_1 \)-value (i.e., 2.5 kΩ, 2 kΩ, 1.5 kΩ, 1 kΩ, and 0.5 kΩ). The values of \( g_m = 0.5 \text{ mA/V} \) and \( C_1 = 0.1 \text{nF} \) are taken to obtain \( R_{\text{eq}} = 2 \text{kΩ} \) for all plots. For a given \( R_1 \), the corresponding \( L_{\text{eq}} \) values are simulated as 0.5 mH, 0.4 mH, 0.3 mH, 0.2 mH, and 0.1 mH, respectively.

Fig. 12. Simulated \( Z_{\text{in1}} \)-magnitude responses with tuning \( R_{\text{eq}} \).
B. Simulation results of the proposed grounded lossy inductance simulator circuit in Fig.4

For the proposed grounded lossy parallel-type inductance simulator circuit of Fig.4, the time-domain and frequency responses for $g_m = 0.5 \text{ mA/V}$, $R_2 = 1 \Omega$ and $C_2 = 0.1 \text{ nF}$ are shown in Fig.14 and 15, respectively. According to (4), the simulated equivalent elements can be realized as $R_{eq} = 1 \Omega$ and $L_{eq} = 0.2 \text{ mH}$. As can be observed from Fig.14, when an input sine-wave signal with 1 MHz and amplitude of 80 mV has been applied, its phase difference is around 38°. In this case, the total power dissipation of the simulated lossy inductor is about 15.3 mW for a given bias condition.

It may also be observed from (4) that the $R_{eq2}$ variation can be accomplished by the adjustment of $R_2$. Moreover, the $R_{eq2}$ tuning can be obtained without affecting $L_{eq2}$ by keeping the $R_2/g_m$ ratio constant. The orthogonal adjustment of $R_{eq2}$ and $L_{eq2}$ is demonstrated in Fig.16 by plotting the $Z_{in2}$-magnitude responses for $R_{eq2} = R_2 = 1 \Omega$, 1.5 kΩ, 2 kΩ and 2.5 kΩ, while keeping $R_2/g_m$ fixed at $2 \times 10^6$. On the other hand, the simulated magnitude responses of $Z_{in2}$ are depicted in Fig.17 for $L_{eq2} = 0.3 \text{ mH}, 0.4 \text{ mH}, 0.5 \text{ mH}$ and $0.7 \text{ mH}$, when $R_{eq2}$ remains constant at 2 kΩ. It is evident from both figures that the simulated equivalent elements $R_{eq2}$ and $L_{eq2}$ can be tuned orthogonally.

VII. APPLICATION EXAMPLES

As the first application of the proposed floating inductance simulator circuit in Fig.3, it was employed to implement a second-order RLC low-pass filter [38], as shown in Fig.18. Routine analysis of the configuration of Fig.18 shows that the voltage transfer function, the pole frequency ($f_p$), and the quality factor ($Q$) are found as:

$$V_{out}(s) = \frac{g_m}{R C_L C_{LP}}$$

where

$$s^2 + \frac{s}{R C_1} + \frac{X}{R C_{LP}} = 0.$$
The electronic tunability of the realized low-pass filter can be assessed by changing the transconductance $g_m$ of the FB-VDBA. The gain-frequency domain behavior with respect to $g_m$ (i.e., $g_m = 0.2$ mA/V, 0.3 mA/V, 0.5 mA/V, and 1 mA/V) is shown in Fig.20. As mentioned in (16) and (17), the ideal pole frequencies are $f_p = 1$ MHz, 1.3 MHz, 1.58 MHz, and 2.25 MHz, and the ideal quality factors are $Q = 0.65, 0.82, 1,$ and 1.41. The total harmonic distortion variations (THD) variation in the filter output is also measured by applying sinusoidal input voltages at 1.58 MHz. The obtained results are plotted in Fig.21, which is observed that the THD remains below 10% for input voltage signal up to 300 mV.

Furthermore, the RLC parallel resonance circuit in Fig.22 is performed to verify the functionality of the proposed grounded inductance simulator circuit of Fig.4. For this purpose, the parallel R and L in the prototype passive circuit is replaced by the simulated parallel RL of Fig.4. The component values are taken as $R_2 = 2$ kΩ, $C_2 = 0.1$ nF and $C_{RES} = 50$ pF, to achieve $R_{eq2} = 2$ kΩ. The simulated plots of the magnitude-frequency characteristic at different $g_m$ values (i.e. 0.28 mA/V, 0.40 mA/V, 0.66 mA/V, and 1 mA/V) are given in Fig.23. This adjustment results in different $L_{eq2}$ values, i.e. 0.7 mH, 0.5 mH, 0.3 mH and 0.2 mH, respectively.
In this article, series and parallel lossy inductance simulating configurations using a fully balanced voltage differencing buffered amplifier (FB-VDBA) are presented. Each present topology utilizes only one FB-VDBA, one resistor, and one capacitor. The tuning of the simulated equivalent elements is realized by adjusting the bias current and/or the resistor in the simulators. As application examples, RLC second-order low-pass filter and parallel resonance circuits are constructed using the proposed inductor circuits. Simulation results are given to verify the functionality of the proposed inductor circuits.

VIII. CONCLUSIONS

In this article, series and parallel lossy inductance simulating configurations using a fully balanced voltage differencing buffered amplifier (FB-VDBA) are presented. Each present topology utilizes only one FB-VDBA, one resistor, and one capacitor. The tuning of the simulated equivalent elements is realized by adjusting the bias current and/or the resistor in the simulators. As application examples, RLC second-order low-pass filter and parallel resonance circuits are constructed using the proposed lossy inductance simulators. Simulation results are given to verify the functionality of the proposed inductor circuits.

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