Single Voltage Differencing Gain Amplifier-Based Dual-Mode Quadrature Oscillator Using Only Grounded Passive Components

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***Abstract*—This article describes the compact quadrature sinusoidal oscillator, which produces both voltage and current quadrature outputs at the same time. By utilizing a voltage differencing gain amplifier (VDGA) as an active element, the proposed dual-mode quadrature oscillator is realized with only three grounded passive elements, namely one resistor and two capacitors. The adjustment rules for the condition of oscillation and the frequency of oscillation are orthogonally controllable by the independent VDGA bias currents. Non-ideal influences on the circuit's behavior are also examined in detail. PSPICE-based computer simulation was used to evaluate the theoretical hypotheses of circuit functioning.**

***Index Terms*—Voltage Differencing Gain Amplifier (VDGA), quadrature oscillator (QO), dual-mode operation, tunable circuit.**

I. Introduction

A sinusoidal quadrature oscillator (QO) that creates two equaled-amplitude outputs with a 90° phase difference is a fundamental circuit block that is used in many signal processing and information systems, such as single-sideband vector generators, quadrature mixers, and selective voltmeters. Numerous QO solutions based on various high-performance active devices have been proposed in the open technical literature over the last few decades [1–21]. A close examination reveals that the QO realizations in [1–8] produced current-mode outputs, whereas the works in [9–21] produced voltage-mode outputs. Also, recall that none of the previously listed oscillator circuits can create both voltage and current signals at the same time. There are a few circuits in the literature that have the benefit of simultaneously providing explicit quadrature voltage and current signals [22–27]. However, these oscillator realizations possess one or more of the following drawbacks: (i) contain two or more active elements [23]-[25]; (ii) include at least four passive components [22], [24]-[27]; (iii) comprise floating passive components [24]; as well as (iv) lack electronic adjustment of their essential parameters [22], [24].

Therefore, this study makes an attempt to present an electrically adjustable sinusoidal QO with both voltage and current quadrature outputs at the same time. The suggested QO circuit is canonic and low-component count, with just one voltage differencing gain amplifier (VDGA), two capacitors, and one resistor. Three passive elements are all grounded, which is favorable for further monolithic implementation. External biasing currents are used to achieve orthogonal electronic control of the condition of oscillation (CO) and the oscillation frequency (ω_o). The characterization operations of the proposed QO have been examined through PSPICE simulation based on 0.35-µm CMOS manufacturing technology.

II. Description of Voltage Differencing Gain Amplifier (VDGA)

The VDGA is a five-terminal versatile analog active building block suggested by J. Satansup and W. Tangsrirat in 2013 [28]. In the literature, certain applications of the VDGA element have been developed, including a voltage-mode biquad filter [28], an nth-order low-pass filter [29], and a sinusoidal oscillator [30]. Fig. 1 depicts the VDGA's symbolic circuit representation. Ignoring the non-idealities of the device used, the ideal behavior of this element may be stated as

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mA} & -g_{mA} & 0 & 0 \\ 0 & 0 & g_{mB} & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ v_x \end{bmatrix} \quad (1)$$

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The VDGA, as defined in the literature, can be realized using a suitable CMOS technology, as illustrated in Fig. 2 [28]. The three floating current sources (FCSs) M_{1A}-M_{9A}, M_{1B}-M_{9B}, and M_{1C}-M_{9C} realize independent programmable transconductance gains of g_{mA}, g_{mB}, and g_{mC} [31]. The expression for the transconductance g_{mk} (k = A, B, C) of the FCS M_{1k}-M_{9k} may well be written by:

$$g_{mk} \cong \left(\frac{g_{1k}g_{2k}}{g_{1k}+g_{2k}}\right)+\left(\frac{g_{3k}g_{4k}}{g_{3k}+g_{4k}}\right) \quad , \tag{2}$$

where $$g_{ik} = \sqrt{KI_{Bk}} \quad \text{for } i = 1, 2, 3, 4 \tag{3}$$

and K is the transconductance coefficient of the device, and I_{Bk} is the external bias current. It may be mentioned that the transconductance g_{mk} can be controlled electronically by utilizing I_{Bk}.

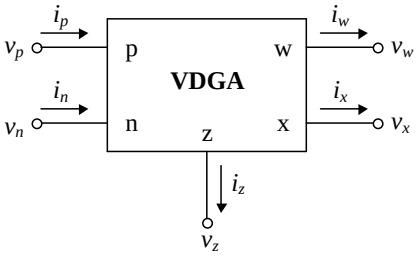


Fig. 1. Circuit symbol for the VDGA

According to Fig.2, the FCS M_{1A}-M_{4A} is a differential-input voltage to current converter with the transconductance g_{mA} (i_z = $g_{mA}(v_p$-$v_n)$), whereas the FCS M_{1B}-M_{4B} converts the voltage v_z into the x-terminal current i_x with the gain g_{mB} (i_x = $g_{mB}v_z$). A pair of FCSs M_{1B}-M_{4B} and M_{1C}-M_{4C} effectively realize a tunable-gain voltage amplifier stage between the w and z terminals (v_w = βv_z). For this circuit, the voltage transfer gain β for this stage is equal to

$$g_m = \sqrt{KI_B} \tag{4}$$

which can be fine-tuned with modifying the g_{mB}/g_{mC} ratio or the I_{BB}/I_{BC} ratio.

In non-ideal conditions, the practical VDGA, including its non-ideal transfer gains, can be modeled as:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_A g_{mA} & -\alpha_A g_{mA} & 0 & 0 \\ 0 & 0 & \alpha_B g_{mB} & 0 \\ 0 & 0 & \delta\beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ v_x \end{bmatrix} \quad , \tag{5}$$

where α_k and δ denote the non-ideal transconductance gain and the non-ideal voltage transfer gain, respectively. Furthermore, when the parasitic impedances at the VDGA's corresponding terminals are taken into account, its non-ideal model is represented in Fig.3. In Fig.3, R_j and C_j (j = p, n, z, x, w) represent to the parasitic resistance and capacitance at the corresponding terminal, respectively.

III. Proposed Dual-Mode QO Circuit

The proposed sinusoidal QO circuit, which is found to possess both the voltage and current quadrature signals at the same time, is depicted in Fig.4. A single VDGA is used as an active element in the realization, along with one grounded resistor and two grounded capacitors. The use of only grounded resistors and capacitors is appropriate for monolithic integration and is also beneficial for absorbing various parasitic impedance effects [32]. Routine circuit analysis of the QO in Fig.4 using (1) yields the following characteristic equation:

$$s^2C_1C_2 + sC_2\left(\frac{1}{R_1} - \frac{g_{mA}g_{mB}}{g_{mC}}\right) + g_{mA}g_{mB} = 0 \quad . \tag{6}$$

The condition and frequency of oscillation (CO and ω_o) can be obtained from (6) as, respectively,

$$g_{mA}g_{mB}R_1 = g_{mC} \quad , \tag{7}$$

and $$\omega_o = 2\pi f_o = \sqrt{\frac{g_{mA}g_{mB}}{C_1C_2}} \quad . \tag{8}$$

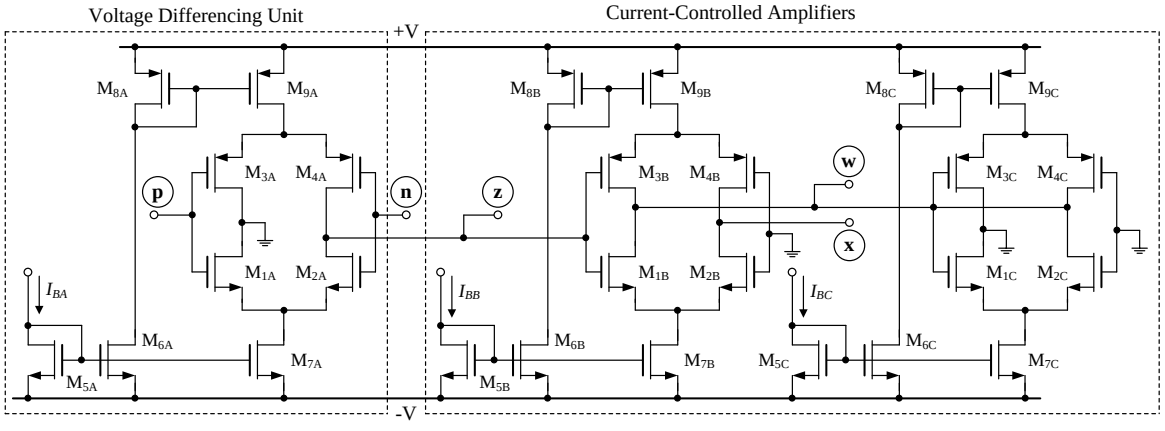


Fig. 2. CMOS realization of the VDGA

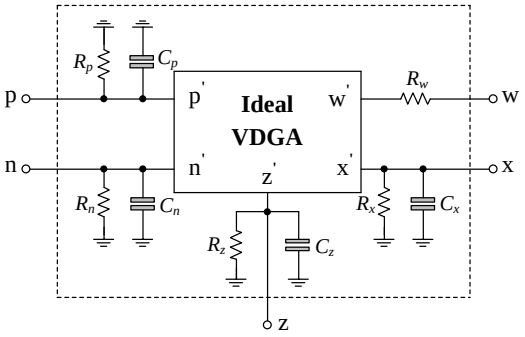


Fig. 3. Practical model of the VDGA device involving parasitic elements

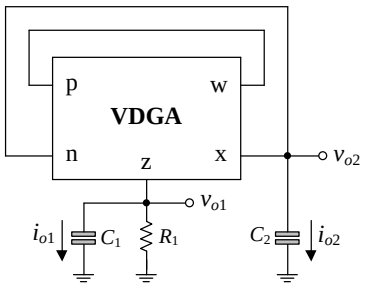


Fig. 4. Proposed dual-mode QO circuit

The formulas above show that CO may be regulated without influencing ω_o by adjusting the regulating g_{mC}. (I_{BC}). The ω_o, on the other hand, may be altered by varying g_{mA} and/or g_{mB}, and therefore by bias currents I_{BA} and/or I_{BB}.

Also from Fig.4, the two explicit quadrature output voltages v_{o1} and v_{o2} are exhibited to form the following relationship:

$$v_{o1} = \left(\frac{j\omega C_2}{g_{mB}}\right) v_{o2} \quad . \tag{9}$$

The two quadrature current outputs marked i_{o1} and i_{o2} are related by the following equation:

$$i_{o1} = \left(\frac{j\omega C_1}{g_{mB}}\right) i_{o2} \quad . \tag{10}$$

It is evident from (9) and (10) that the two outputs will be 90° out of phase, proving the circuit is quadrature property. As a result, the proposed circuit is versatile since it has both voltage and current quadrature outputs to provide dual-mode operation.

IV. Non-Ideal Gain Effects and Sensitivity Calculations

Taking into consideration the VDGA non-idealities indicated in (5), the characteristic parameters CO and ω_o are modified as follows:

$$\delta \alpha_A g_{mA} g_{mB} R_1 = g_{mC} \quad , \tag{11}$$

and

$$\omega_o = \sqrt{\frac{\alpha_A \alpha_B g_{mA} g_{mB}}{C_1 C_2}} \quad . \tag{12}$$

It is apparent that the VDGA's non-ideal transfer gains directly influence the values of CO and ω_o. To adjust for variances in the CO and ω_o-values, simply tune over the CO and ω_o through the transconductances g_{mC}, and g_{mA} and/or g_{mB}, respectively.

According to (12), the relative sensitivity investigation of ω_o in relation to different circuit components reveals that

$$S_{\alpha_A}^{\omega_o} = S_{\alpha_B}^{\omega_o} = S_{g_{mA}}^{\omega_o} = S_{g_{mB}}^{\omega_o} = \frac{1}{2} \quad , \tag{13}$$

and

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2} \quad . \tag{14}$$

Evidently from (13) and (14), all the ω_o-sensitivity coefficients have a magnitude of 0.5. As a result, the proposed QO circuit in Fig.4 has a low sensitivity performance.

V. Effects of VDGA Parasitics

Following Fig.3, Fig.5 depicts the practical small-signal behavior of the proposed QO circuit in Fig.4, incorporating VDGA parasitic impedances. Thus, taking these parasitics into effect the non-ideal parameters CO and ω_o are modified as follows:

$$g_{mA} g_{mB} = g_{mC} \left[\frac{1}{(R_1 // R_z)} + \frac{(C_1 // C_z)}{(R_n // R_x)(C_2 // C_n // C_x)} \right] \quad , \tag{15}$$

and

$$\omega_o = \sqrt{\left(\frac{g_{mA} g_{mB}}{C_1 C_2}\right)\left[1 - \frac{1}{g_{mC}(R_n // R_x)}\right]} \quad . \tag{16}$$

Considering ($R_1 << R_z$), ($C_1 >> C_z$) and ($C_2 >> C_n$, C_x), then (15) and (16) can be estimated as, respectively,

$$g_{mA} g_{mB} = g_{mC} \left[\frac{1}{R_1} + \frac{C_1}{R_2' C_2} \right] \quad , \tag{17}$$

and

$$\omega_o = \sqrt{\left(\frac{g_{mA} g_{mB}}{C_1 C_2}\right)\left[1 - \frac{1}{g_{mC} R_2'}\right]} \quad . \tag{18}$$

where $R_2' = (R_n // R_x)$. According to (17), the parasitic impedances have a detrimental effect on the CO for identical values of capacitances C_1 and C_2 and for $R_1 << R_n // R_x$. Equation(18) demonstrates that the parasitic resistances R_n and R_x cause the ω_o to diverge from its ideal value. For example, if $g_{mA} = g_{mB} = g_{mC} = 380$ μA/V, $C_1 = C_2 = 10$ pF, $R_n = 500$ kΩ, and $R_x = 265$ kΩ, the ω_o-value percentage variation is 0.76%.

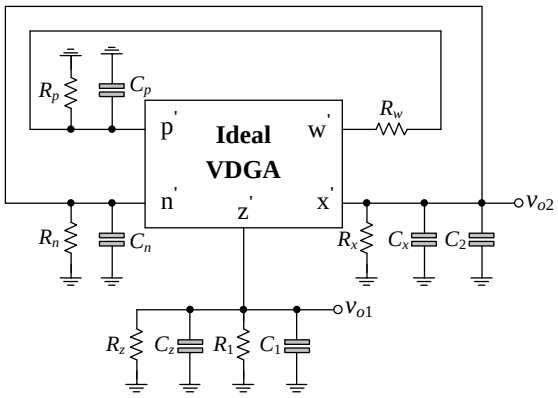


Fig. 5. Practical model of the proposed QO.

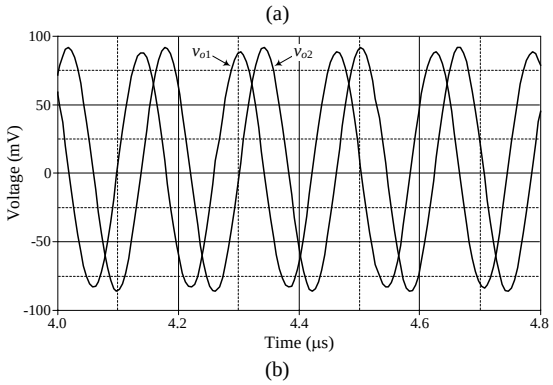


Fig. 6. Simulated time-domain responses for v_{o1} and v_{o2} of the proposed voltage-mode QO in Fig.4. (a) Transient waveforms (b) Steady-state waveforms

VI. Simulation Results and Performance Discussions

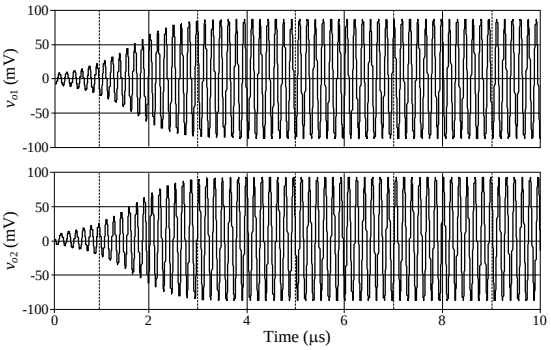
The PSPICE simulator has been used to investigate the behavior of the proposed dual-mode QO in Fig. 4. The CMOS implementation of the VDGA of Fig.2 was performed in simulations employing 0.35-mm TSMC CMOS process parameters and 1.5V supply voltages. Table I provides the geometrical transistor sizes.

TABLE I
GEOMETRICAL TRANSISTOR SIZES OF CMOS VDGA IN FIG.2.

Transistors	W/L (μm/μm)
$M_{1k} - M_{2k}$	22/0.25
$M_{3k} - M_{4k}$	24/0.25
M_{5k}	5/0.25
$M_{6k} - M_{7k}$	4.5/0.25
$M_{8k} - M_{8k}$	5.8/0.25

The VDGA-based dual-mode QO circuit in Fig.4 was designed for $f_o \cong 6.08$ MHz. The computed component values for $C = C_1 = C_2 = 10$ pF were derived from (7) and(8) as follows: $g_m = g_{mk} \cong 382$ μA/V (for $I_B = I_{Bk} = 40$ μA) and $R_1 = 2.6$ kΩ. Figs. 6 and 7 show the simulated transient responses for the quadrature voltage outputs (v_{o1} and v_{o2}) and current outputs (i_{o1} and i_{o2}). In both cases, the corresponding f_o was measured to be around 6 MHz, with a percentage error of 1.32%.

Furthermore, as seen in Figs. 6 and 7, the quadrature oscillation outputs deviate in phase by 89° for voltage-mode operation and 86° for current-mode operation. It is also discovered that for the specified component values, the overall power consumption of the circuit is roughly 1.36 mW.



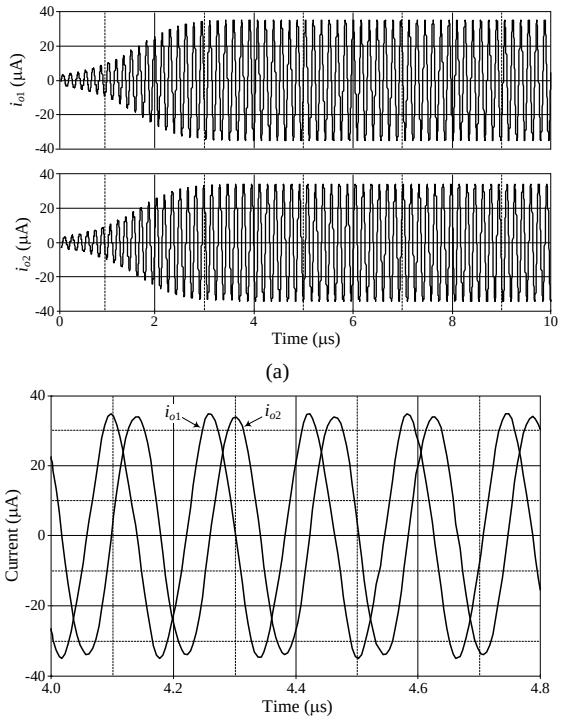


Fig. 7. Simulated time-domain responses for i_{o1} and i_{o2} of the proposed voltage-mode QO in Fig.4. (a) Transient waveforms (b) Steady-state waveforms

The Lissajous figures of the two output voltages and currents are shown in Fig. 8 to find out the correlation between the quadrature outputs. The simulated frequency spectrums at f_o for both output waveforms are also shown in Fig. 9. The total harmonic distortion (THD) values at the voltage and current output waveforms are almost 3.25% and 3.36%, respectively.

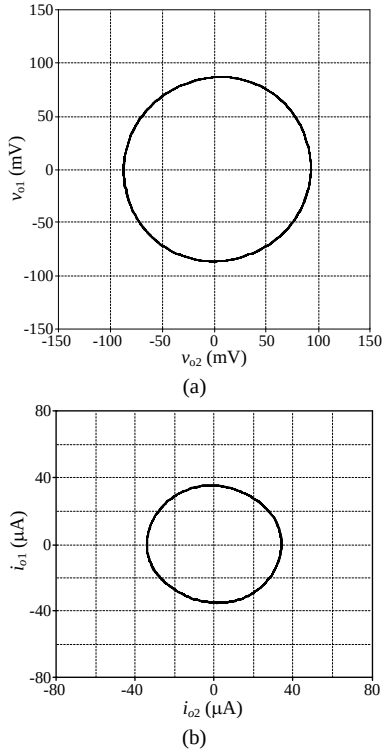


Fig. 8. Lissajous figures at f_o showing quadrature property.
(a) for v_{o1} and v_{o2} (b) for i_{o1} and i_{o2}.

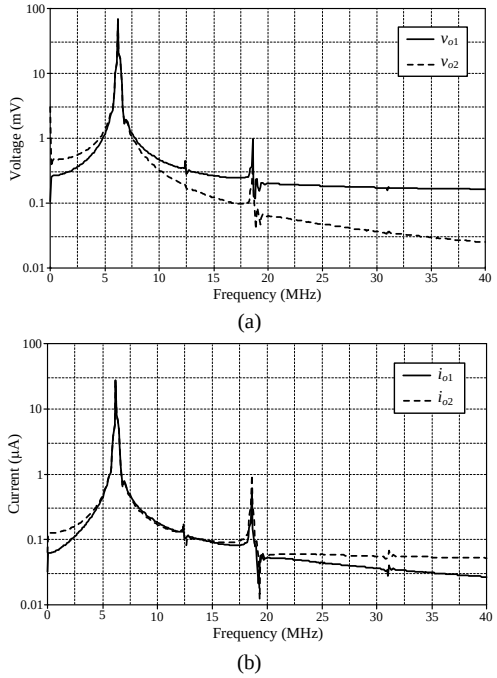


Fig. 9. Frequency spectrums at f_o
(a) for v_{o1} and v_{o2} (b) for i_{o1} and i_{o2}

The electronic adjustability of the oscillation frequency f_o by tuning g_m is shown in Fig. 10 for C= 10 pF, 0.1 nF, and 1 nF. In the high bias current value range, a discrepancy between the simulated and calculated values is observed. This little discrepancy can be mitigated by fine-tuning the value of I_B.

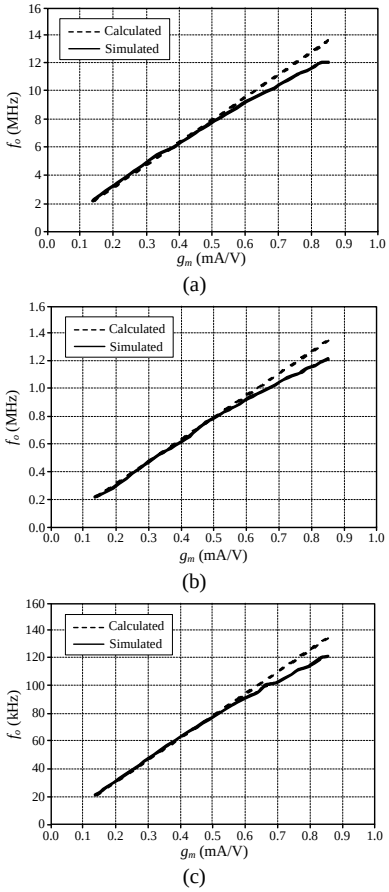


Fig. 10. Variation of f_o with g_m
(a) for C = 10 pF (b) for C= 0.1 nF (c) for C = 1 nF

VIII. Conclusions

The dual-mode sinusoidal QO with a single VDGA and all three grounded passive components is detailed in this paper. Without modifying the circuit architecture, the oscillator circuit may produce both quadrature voltage and quadrature current outputs at the same time. All of the passive components used in this implementation are grounded. By adjusting the bias currents of the VDGAs, the condition and frequency of oscillation may be adjusted orthogonally and electronically. PSPICE simulation findings corroborate the theoretical expectations.

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