A Full Integrated Gain Variable LNA for WCDMA

Zhi-Ming Lin and Yu-Chun Huang, *Member, IAENG*

***Abstract*—In this paper we propose a gain-variable low noise amplifier (LNA) for low-voltage and low power WCDMA application. The LNA is designed based on a current-reused topology and a variable gain circuit. The test chip is simulated and fabricated with the TSMC 0.18 μm CMOS process. Experimental results show that the LNA exhibits 20 dB of gain, 3.5 dB of noise figure and -12dB of input return loss (S11), and -7dB of output return loss (S22) while consuming a DC power of 3.2 mW from a 1V supply voltage. Due to the operation for low-voltage and low-power environment, the attained IIP3 is -12.5dBm and P1dB is -19dBm. The variable gain range is from 19.75 to 11.25 dB.**

***Index Terms*—WCDMA, low noise amplifier (LNA), RF, variable gain.**

I. INTRODUCTION

The advances in the modern CMOS technologies raise the operating frequency in RF CMOS designs and make the fully integration of communication system realizable. In the receiver chain of a communication system, a low noise amplifier (LNA) is the first stage dominating the noise and sensitivity performance of the communication system. The LNA is the block entrusted to amplify the weak signal received by the antenna in a reception system. Typically, high-gain and low-noise implementation of LNA involves high power dissipation, which is not a desirable option with portable wireless system. In this paper, we propose a gain-variable LNA for low-voltage and low power operation on a current-reused topology. The following section introduces the chosen low voltage topology, and we try to find out the best value of noise figure (NF) and aspect ratios of MOSFET transistors for the LNA.

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Z. M. Lin is with the National Changhua University of education, Graduate Institute of Integrated Circuit Design (corresponding author to provide phone: (04)7232105-7862; fax: 04-7211258; e-mail: zmlin@cc.ncue.edu.tw).

Y. C. Huang was with National Changhua University of education, Department of Electrical Engineering (e-mail: anb74dk@yahoo.com.tw).

II. NOISE ANALYSIS OF MOS TRANSISTOR

In the case of LNA, however, not only sufficient gain is needed to overcome the noise for the next mixer, but also a good noise performance is required as well. The noise model of MOSFET is shown in Fig. 1. It concludes several main noise sources: channel thermal noise ($\overline{i_d^2}$), gate induced noise ($\overline{i_g^2} \equiv \overline{i_{g,c}^2} + \overline{i_{g,u}^2}$), the noise due to the gate resistor ($\overline{i_{\mathrm{rg}}^2}$).

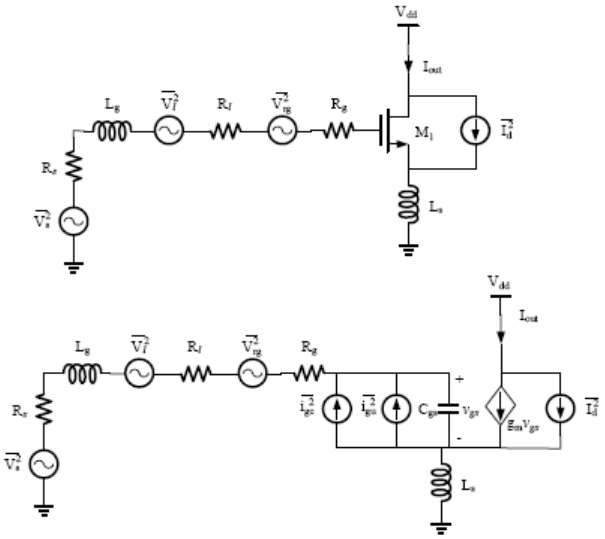

Fig. 1. Equivalent circuit of MOS noise calculation for input stage.

A. Channel Thermal Noise ($\overline{i_d^2}$)

$\overline{i_d^2} = 4kT\gamma g_{do}\Delta f$, where g_{do} is the zero-bias drain conductance of the device, Δf is noise bandwidth, k is the Boltzman constant, T is the absolute temperature and γ is a bias-dependent factor that, for long-channel devices, satisfies the inequality $\frac{2}{3} \le \gamma \le 1$. For short-channel devices, γ may be as high as two to three, depending on bias conditions [1]. For instance, γ is 2.5 in typical 0.18 μm TSMC 1p6m CMOS technology.

B. Gate Induced Noise ($\overline{i_g^2} \equiv \overline{i_{g,c}^2} + \overline{i_{g,u}^2}$)

The gate induced noide can be expressed as

$$\begin{aligned}\overline{i_g^2} &= 4kT\delta g_g \Delta f = \overline{i_{g,c}^2} + \overline{i_{g,u}^2} \\ &= 4kT\delta g_g (1-|c|^2)\Delta f + 4kT\delta g_g |c|^2 \Delta f\end{aligned} \tag{1}$$

Where, δ is the coefficient of gate induced noise and shunt conductance $g_g = \frac{\omega^2 C_{gs}^2}{5g_{do}}$ [1]. The denoted *c* and *u* represent correlated and uncorrelated gate induced noise with channel thermal noise respectively. The value of *c* is about 0.395J for long channel device, but c=0.47J in typical TSMC 0.18 μm 1p6m CMOS technology.

C. Gate Resistor Noise ($\overline{i_{rg}^2}$)

The noise of gate resistor can be eliminated by using multi-finger device to form a smaller resistance that can be ignored.

D. Noise Analysis

The noise factor for an amplifier is defined as

$$F = \frac{Total\ output\ noise}{Total\ output\ noise\ due\ to\ the\ source} \tag{2}$$

To estimate the output noise, the first work is the evaluation of the transconductance of the input stage.

$$G_m = g_{m1} Q_{in} = \frac{g_{m1}}{\omega_0 C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{\omega_0 L_s (1 + \frac{\omega_T L_s}{R_s})} \tag{3}$$

Using (3), the output noise power density due to the source is

$$\begin{aligned}S_{a,source}(\omega_0) &= \frac{\overline{i_{o,Vs}^2}}{\Delta f}(\omega_0) = \frac{\overline{V_s^2}}{\Delta f}(\frac{i_o^2}{V_s^2}) = \frac{\overline{V_s^2}}{\Delta f} G_m^2 = \\ & 4KTR_s G_m^2 = \frac{4KT\omega_T^2}{\omega_0^2 R_s (1 + \frac{\omega_T L_s}{R_s})^2}\end{aligned} \tag{4}$$

Similarly, the output noise power density due to R_l and R_g can be expressed as

$$S_{a,R_l,R_g}(\omega_0) = \frac{4kT(R_l + R_g)\omega_T^2}{\omega_0^2 R_s^2 (1 + \frac{\omega_T L_s}{R_s})^2} \tag{5}$$

The output noise power density due to channel current noise of MOSFET is

$$S_{a,i_d}(\omega_0) = \frac{\frac{i_d^2}{\Delta f}}{(1 + \frac{\omega_T L_s}{R_s})^2} = \frac{4kT\gamma g_{d0}}{(1 + \frac{\omega_T L_s}{R_s})^2} \tag{6}$$

The induced drain noise is the combinations of a correlated and an uncorrelated gate induced noise. The combined power density of drain noise with correlated gate induced noise is

$$S_{a,i_d,i_{gc}}(\omega_0) = \kappa S_{a,i_d}(\omega_0) = \frac{4kT\gamma\kappa g_{d0}}{(1 + \frac{\omega_T L_s}{R_s})^2} \tag{7}$$

where

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + [1 + |c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}]^2 \tag{8}$$

$$Q_L = \frac{\omega_0(L_s + L_g)}{R_s} = \frac{1}{\omega_0 R_s C_{gs}} \tag{9}$$

$$C_{gs} = \frac{2}{3} WLC_{ox} \tag{10}$$

The uncorrelated gate induced noise power density is

$$S_{a,i_d,i_{gu}}(\omega_0) = \xi S_{a,i_d}(\omega_0) = \frac{4kT\gamma\xi g_{d0}}{(1 + \frac{\omega_T L_s}{R_s})^2} \tag{11}$$

where

$$\xi = \frac{\delta\alpha^2}{5\gamma}(1 - |c|^2)(1 + Q_L^2) \tag{12}$$

Hence the noise power density of M1 is

$$S_{a,M1}(\omega_0) = \chi S_{a,i_d}(\omega_0) = \frac{4kT\gamma\chi g_{d0}}{(1 + \frac{\omega_T L_s}{R_s})^2} \tag{13}$$

where

$$\chi = \kappa + \xi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L^2) \tag{14}$$

Putting (4), (5), (13) into (2), the noise factor of M_1 is

$$\begin{aligned}F &= \frac{S_{a,source}(\omega_0) + S_{a,R1,Rg}(\omega_0) + S_{a,M1}(\omega_0)}{S_{a,source}(\omega_0)} \\ &= 1 + \frac{R_1}{R_s} + \frac{R_g}{R_s} + \gamma\chi g_{d0} R_s (\frac{\omega_0}{\omega_T})^2\end{aligned} \tag{15}$$

$$g_{d0} Q_L = \frac{g_m}{\alpha} \frac{1}{\omega_0 R_s C_{gs}} = \frac{\omega_T}{\alpha\omega_0 R_s} \tag{16}$$

Substitute (14) into (15), we can express (15) as

$$F = 1 + \frac{R_1}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}(\frac{\omega_0}{\omega_T}) \tag{17}$$

The coefficient χ according to (14) includes terms which are constant and terms which are proportional to Q_L^2. From (17), we see the noise figure will contain terms which proportional to Q_L and terms which are inversely proportional to Q_L. Therefore, a minimum F exists for a particular Q_L [2].

III. Noise Figure Optimization Technique

Choosing MOS size is very important to the LNA design. One primary interest is picking the appropriate device width and bias point to optimize noise performance for given specific objectives on gain and power dissipation. Assume that I_d has the form [3]

$$I_d = WC_{ox}V_{sat}\frac{V_{od}^2}{V_{od}+L\varepsilon_{sat}} \tag{18}$$

with

$$V_{od} = V_{gs} - V_t \tag{19}$$

where C_{ox} is the gate oxide capacitance per unit area, v_{sat} is the saturation velocity, and ε_{sat} is the velocity saturation field strength. We can differentiate this expression to determine the transcondutance, yielding

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \mu_n C_{ox}\frac{W}{L}V_{od}\left[\frac{1+\rho/2}{(1+\rho)^2}\right] \tag{20}$$

$$\rho = \frac{V_{od}}{L\varepsilon_{sat}}\quad \alpha = \frac{1+\rho/2}{(1+\rho)^2} \tag{21}$$

where μ_n is the field-limited electron mobility.

Using (18), we can formulate the power consumption of the amplifier as follows:

$$P_D = V_{dd}I_d = V_{dd}WC_{ox}v_{sat}\frac{V_{od}^2}{V_{od}+L\varepsilon_{sat}} \tag{22}$$

Using (22), (9) and (10), we can relate Q_L to P_D with

$$Q_L = \frac{P_0}{P_D}\frac{\rho^2}{1+\rho} \tag{23}$$

$$P_D = \frac{3}{2}\frac{V_{dd}v_{sat}\varepsilon_{sat}}{\omega_0 R_s} \tag{24}$$

With (20) and (21), we can re-express ω_T as

$$\omega_T \approx \frac{g_m}{C_{gs}} = \frac{g_m}{\frac{2}{3}WLC_{ox}} = \frac{3}{2}\frac{\alpha\mu_n V_{od}}{L^2} = \frac{3\alpha\rho v_{sat}}{L} \tag{25}$$

We can draw on (20), (23) and (25) and substitute into (17). The noise figure can be shown as

$$F = 1 + \frac{\gamma\omega_0 L}{3V_{sat}}P(\rho, P_D) \tag{26}$$

The $P(\rho, P_D)$ can be simplified by assuming $\rho << 1$, then

$$P(\rho, P_D) \approx \frac{\frac{P_D}{P_0}(1+\frac{\delta}{5\gamma}) + 2|c|\sqrt{\frac{\delta}{5\gamma}}\rho^2 + \frac{P_0}{P_D}\frac{\delta}{5\gamma}\rho^4}{\rho^3} \tag{27}$$

Finally, the optimum width of MOSFET can be obtain by

$$W_{M_1,P_D} = \left[\frac{2}{3}\omega_0 LC_{ox}R_s Q_L\right]^{-1} \tag{28}$$

IV. Circuit Topology and Design Concepts

LNA is typically the first stage of the receiver, whose main function is to provide enough gain to overcome the noise of subsequent stages. Thus the noise figure of the LNA is the dominant parameter. At the beginning, the received signal is very small. The LNA offers the highest gain and lowest noise figure in its *high gain mode* for the weak signal. But under strong received signal conditions the LNA and the whole receiver gets saturated and hence the linearity (IIP3) specification also needs to be meet. To satisfy the linearity requirement the proposed LNA operates in the *low gain mode* under strong signal conditions. Therefore, we add a variable resistance attenuator to complete the gain-variable mechanism. The current-reused topology, minimizing noise figure, and resistance-variable attenuator will be discussed in the following.

A. Current-reused topology

The schematic of the LNA with all on-chip components is shown in Fig. 2. With M_1 and M_2 sharing the same bias current, the total power consumption of the current-reused amplifier is minimized. To achieve higher gain than a conventional cascade LNA, both M_1 and M_2 are in common-source configurations. The design considerations of the current-reused LNA are similar to those of a cascaded amplifier [4] [5]. In Fig. 2 the input matching network is composed of C_1, L_1 and R_1 to match the input impedance being 50 Ω. In addition, L_2 and C_3 are also used as the inter-stage between M_1 and M_2. The output matching network is composed of L_3, C_6 and C_5 to easily match the output impedance being 50 Ω.

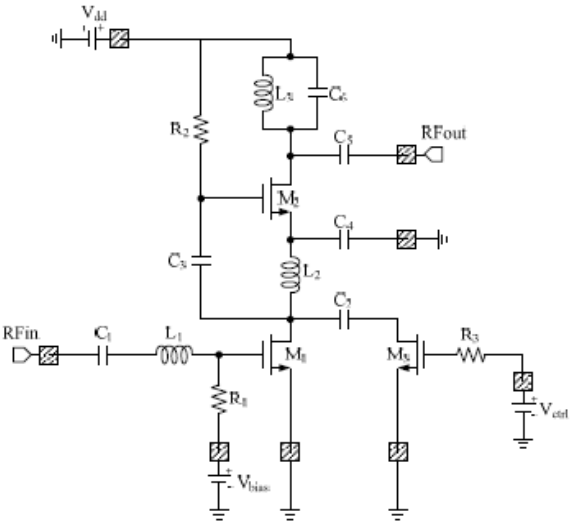

Fig. 2. Designed circuit of the low noise amplifier.

B. MOSFET Device Selection

In order to determine the width of M_1 and find out the best NF, we uses the dependency among F (noise factor), P_D (power dissipation), and Q_L as shown in equations (22) to (28) to find the optimum value. Based on these parameters, the related curves, NF (dB) versus W_{opt} (mm), are plotted in Fig. 3 by MATLAB simulation software. In this figure, we see that the

NF will decrease in the beginning and increase finally as the width of MOSFET increases and the P_D is fixed. According to the simulation results, we choose the W_{opt}, which is located on the nearby minimum NF but a little left shift. We select the P_D as 5mW and the NF as 1.6dB.

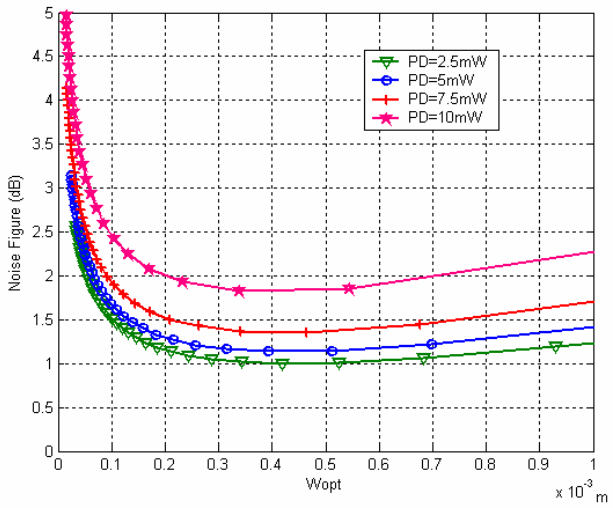

Fig. 3. The related charts of NF, P_D, and W_{opt}.

C. *Resistance-variable attenuator*

The resistance-variable attenuator in Fig. 2 is to include M_3, C_2 and R_3. We make the MOSFET as a variable resistance by controlling the gate voltage. However, large signal will cause a serious inter-modulation problem. A gain-controllable system is added to suppress this phenomenon. The design concept of the resistance-variable attenuator is to use the applied voltage to control the conduction channel of the MOSFET [6]. When the conduction channel is changed, the magnitude of the resistance is also changed. Based on the variable resistance, we can present a gain-controllable function. Besides, the capacitor C_2 is used to isolate the unwanted dc current from the second stage and to maintain the gain-variable function.

V. Results

The microphotograph of the WCDMA LNA, fabricated in a TSMC 0.18 μm standard CMOS technology, as shown in Fig. 4. The measured vs. simulated S-parameters of the LNA is shown in Fig. 5 to Fig. 7. The center frequencies of S11 and S22 are slightly shifted to lower frequency. However, it can still achieve -12dB S11 and -7dB S22 at 2.14GHz. The forward gain of LNA is 20dB at 2.14GHz. The measured results are close to the simulated result. The measured noise figure of the LNA is shown in Fig. 8. The LNA achieves a noise figure of 3.5dB.

The measured gain is shown in Fig. 9. An input referred 1dB compression point is -19 dBm. A two tone test IIP3 measurement was performed on the LNA and the results are shown in Fig. 10. The two tones were applied with equal power levels at 2.14 GHz and 2.145 GHz. The measurement indicates a -12.5dBm input-referred third order intercept point. The variable gain is ranged from 19.75 to 11.25 dB as shown in Fig. 11.

After re-simulation, we found the connecting metal line is too long that will increase inductance value and shift the central frequency of the LNA so that the measurement results do not match with the expected data. The performance of this LNA is summarized in Table I, together with other works for comparison. At low-voltage supply, the power consumption is smaller than the other references and the power gain are better than that reported in [7] and [9]. This circuit achieves high-gain and low-noise for low-voltage and low power operation.

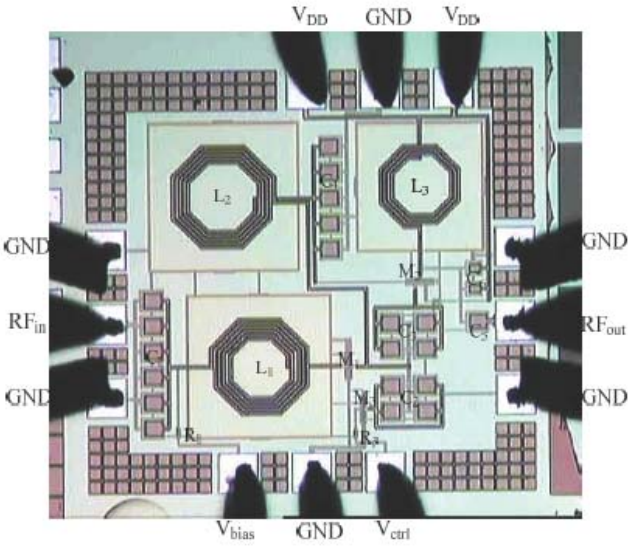

Fig. 4. Microphotograph of the LNA.

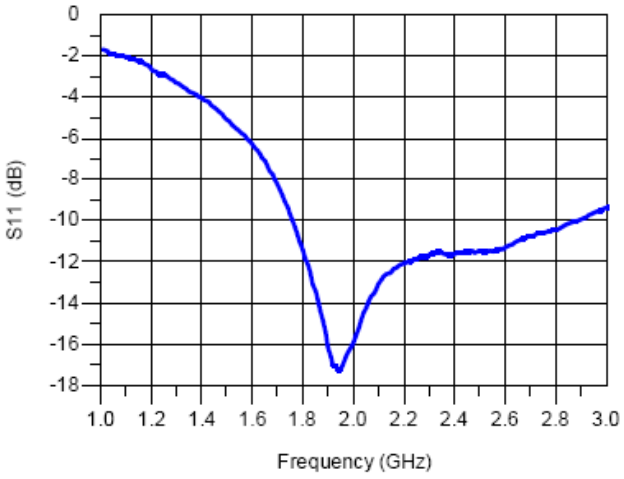

Fig. 5. Measured S11 of the LNA.

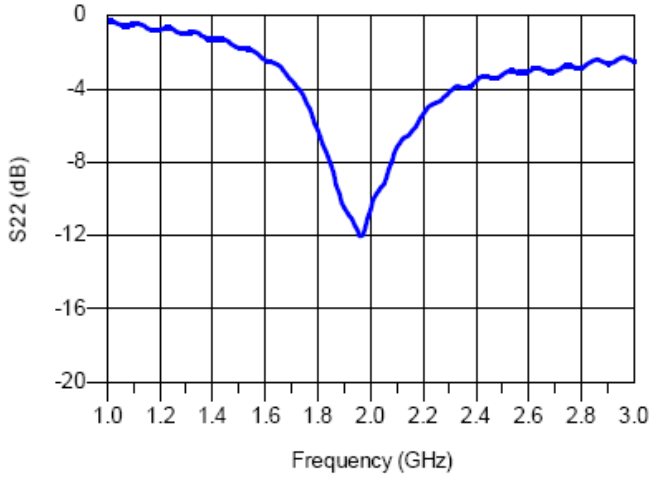

Fig. 6. Measured S22 of the LNA.

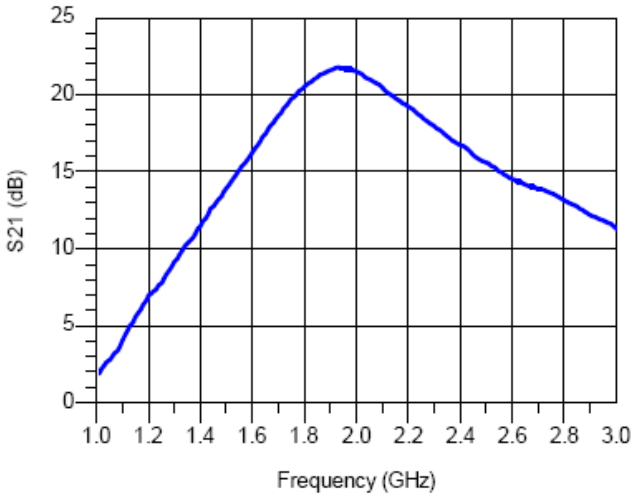

Fig. 7. Measured S21 of the LNA.

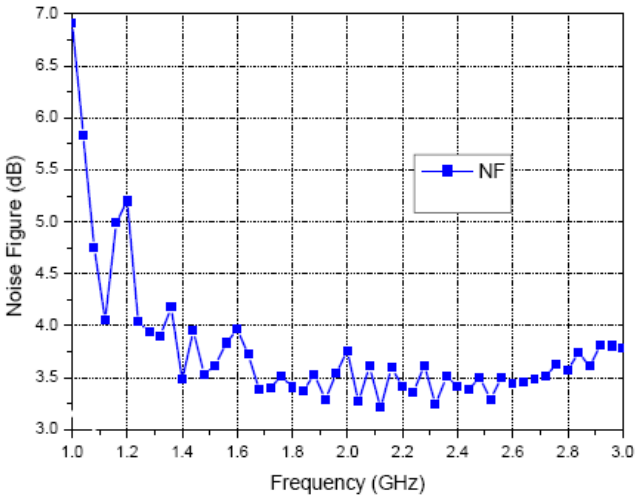

Fig. 8. Measured noise figure of the LNA.

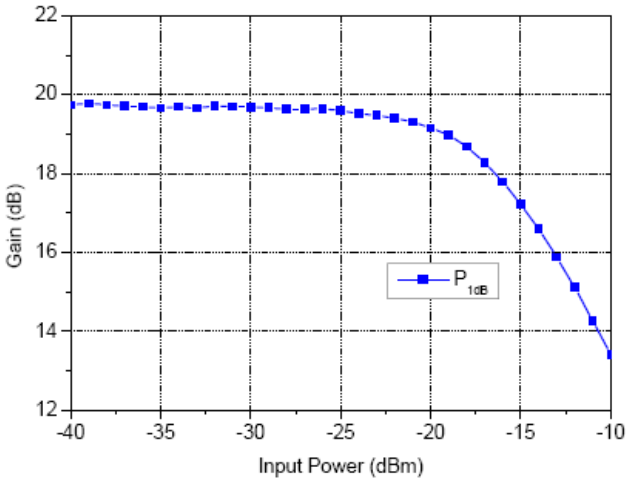

Fig. 9. Measured gain of the LNA.

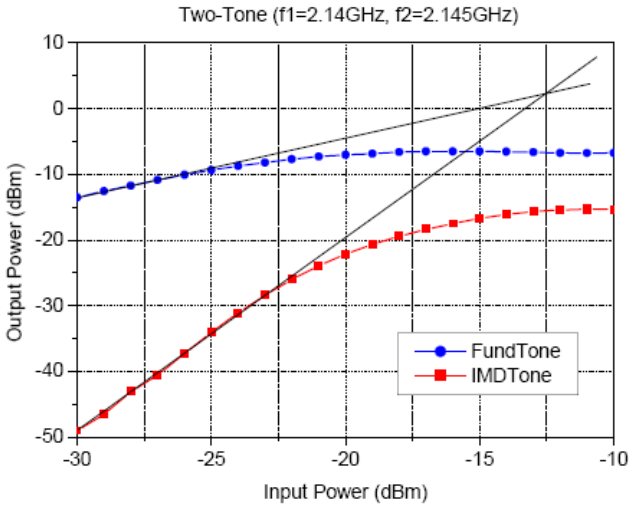

Fig. 10. Measured IIP3 of the LNA.

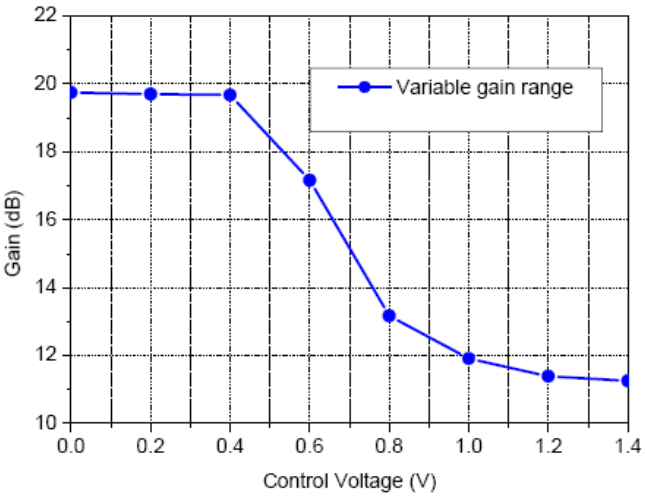

Fig. 11. Measured variable gain range of the LNA.

Table I Performance comparison of LNAs

Reference	This Work (measured)	[7]	[8]	[9]
Frequency [GHz]	2.14	2.1	2.4	2.4
Technology [μm]	0.18	0.13	0.18	0.18
Power Gain [dB]	20	12	23	9.85
NF [dB]	3.5	2.3	3.8	3.23
P_{1dB} [dBm]	-19	-12	-	-
IIP3 [dBm]	-12.5	-5.4	-9.1	-1
Power consumption [mW]	3.2	9.75	13	9.85

VI. Conclusions

The low-power gain variable LNA with current-reused topology is designed and fabricated in a standard 0.18μm CMOS technology. The WCDMA LNA exhibits 20 dB gain, 3.5 dB noise figure while consuming a DC power of 3.2 mW from a 1 V supply. It demonstrates the potential of CMOS RF designs for low-power and low-voltage applications at WCDMA system.

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Zhi-Ming Lin (S'88–M'91) was born in Taiwan, R.O.C. He received the B.S. degree from the National Taiwan Normal University, Taipei, Taiwan, R.O.C., in 1980, the M.S. degree from the National Ching Hua University, Hsin Chu, Taiwan, R.O.C., in 1983, and the Ph.D. degree in electrical engineering from the University of Maryland, College Park, in 1991.

In 1992, he joined the Department of Electrical Engineering, Kaohsiung Institute of Technology, Kaohsiung, Taiwan, R.O.C. In 1994, he joined the National Changhua University of Education, Changhua, Taiwan, R.O.C., where he is currently a Professor and Chief in the Graduate Institute of Integrated Circuit Design. His research interests include very large scale integration/computer aided design.