

# Selective Harmonic Elimination Using Genetic Algorithm for Multilevel Inverter with Reduced Number of Power Switches

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**Abstract**—Multilevel inverters have been widely used in the power applications to get low total harmonic distortion (THD) in medium or high voltage levels. There have been several techniques that can be applied to multilevel inverter so as to get low THD in the output voltage. Selective Harmonic Elimination (SHE) technique is one of these techniques and also has an extensive field of applications in power electronics. It is also an alternative to usual PWM techniques and includes nonlinear equations of stepped voltage waveform. In addition, SHE technique offers to control effective value of output voltage. In this paper, multilevel inverter with reduced number of switches which enables a reduction in the system cost has been proposed, and solution of nonlinear SHE equations have been optimized by Genetic Algorithm (GA) software. The results of simulation and analysis have clearly demonstrated that proposed GA based SHE technique can eliminate desired harmonic order.

**Index Terms**—Genetic algorithm, multilevel inverter, reduced number of switches, selective harmonic elimination, total harmonic distortion

## I. INTRODUCTION

IN recent years, power converters applications in industry have increased due to the developments in semiconductor technology and the different pulse width modulation techniques. Especially, in high power and medium voltage applications, multilevel inverter topology has come up with a choice because power switches which withstand the medium voltage have not been developed with available technology yet [2].

Multilevel inverters generating output voltage in the form of stepped wave was presented in 1975, firstly. This form of the inverter has included the series connection of H-bridge. After that, the structures of the diode clamped multilevel inverter and the capacitor clamped multilevel inverter have been developed, respectively [2], [3]. Diode clamped structure requires clamped diodes the number of which increases exponentially with rising level. Thus, it is not convenient to implement especially in high level applications. Similarly, a great number of clamped capacitor

needed in capacitor clamped structure make the system impractical to implement. Therefore cascaded H-bridge topology is used in high level number [1], [4].

Multilevel inverter has superior performances such as lower  $dv/dt$  for good electromagnetic compatibility, reduced voltage stress on the switches, input current with low distortion, more importantly having lower total harmonic distortion than traditional two-level inverter in output voltage and currents [2], [5], [6]. By applying the different techniques aiming at the elimination of harmonics, the THD of multilevel inverter's output voltage can be decreased. One of the most important techniques is Selective Harmonic Elimination (SHE) method that can eliminate the desired any harmonic content. At the first stage, the nonlinear equations of output voltage harmonics including trigonometric terms must be obtained. In the second stage, which is the basic purpose of SHE technique, switching angles can be acquired with solving the harmonic equations. These equations change according to the number of harmonics' order desired to eliminate and the requested output voltage value [1], [5], [6].

The usual methods to obtain switching angles are iterative and analytical methods such as Newton-Raphson [7], Symmetric Polynomials and Groebner Bases Theory. The iterative methods are sensible to the initial value and divergence problems are probably to arise, also the optimal switching angles may not be produced for the minimum THD [8]. These methods are time-consuming and also provide complex solution due to the necessity of different look-up tables for each modulation indexes [9], [10]. The other methods to calculate switching angles are artificial intelligence approaches such as GA and Particle Swarm Optimization (PSO). The GA gives the optimum solution of the harmonic equations in contrast to the iterative methods [11], [12]. In addition researchers have compared GA and PSO in [13], and demonstrated that GA solves harmonic equations by taking less computational time.

Multilevel inverters have several disadvantages. The most significant drawback is the necessity of great number of switches. In addition, the drivers of each level module must be isolated from each other. As THD decreases with rising level, the hardware of multilevel inverter needs more isolated power source. That leads the increasing expense of inverter according to conventional inverter. Thus, to realize the lower cost applications, it is very important to reduce the number of power semiconductor switches and drivers [2], [11]. Many studies working on reducing of number of components MLI's structure have been done in [2], [3]. This

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paper presents not only reducing of power components in MLI but also implementing of SHE techniques to proposed MLI with reduced number of switches. In addition proposed multilevel inverter structure resembles cascaded multilevel inverter with H-bridge modules given in [4] and does not require extra clamped diodes or clamped capacitor.

In this paper, multilevel inverter with reduced number of switches using the isolated DC sources has been proposed. SHE equations of the stepped output voltage have been solved by genetic algorithm software which eliminates desired harmonics order without the use of GA toolbox of MATLAB. The results of simulation have clearly proved that the proposed SHE technique for multilevel inverter with reduced number of switches can eliminate the desired harmonics' order [1].

## II. PROPOSED MULTILEVEL INVERTER STRUCTURE

The proposed cascaded multilevel inverter consists of level module units having half-bridge topology with two switches. Each half-bridge is connected isolated DC power supply as shown in Fig. 1. The overall structure of suggested topology includes two basic parts. The first part is the level module units producing DC voltage levels. The second is the H-bridge generating positive and negative stepped output voltage. Regarding isolated DC voltage sources' number is  $k$ , also the number of level-modules, the maximum and minimum rates of level's output voltage are

$$V_{o\_min} = 0 \quad (1)$$

$$V_{o\_max} = kV_{dc} \quad (2)$$

The multilevel inverter is known as symmetric multilevel if all voltage sources equal to  $V_{dc}$  [3]. The number of output voltage levels in symmetric multilevel inverter is

$$N_{level} = 2k + 1 \quad (3)$$

Maximum and minimum rates of load voltage are

$$V_{L\_min} = -kV_{dc} \quad (4)$$

$$V_{L\_max} = +kV_{dc} \quad (5)$$

The number of switches is  $4k$  in H-bridge inverter topology. But in the suggested topology, this value is  $2k+4$ . When compared usual cascaded multilevel inverter and suggested topology in terms of switches' number, suggested topology is more advantageous in multilevel inverter with more than level number 5 (7, 9, ...) [1].

In these types of inverter, in order to get sinusoidal output voltage, switching angles have been calculated analytically by (6) and (7) [2]. This technique aiming sinusoidal output voltage is named as SPWM (Sinusoidal Pulse Width Modulation).

$$N_\alpha = k = \frac{N_{level} - 1}{2} \quad (6)$$

$$\alpha_i = \sin^{-1} \left( \frac{2i-1}{N_{level}-1} \right) \quad i = 1, 2, 3, \dots, k-1, k \quad (7)$$

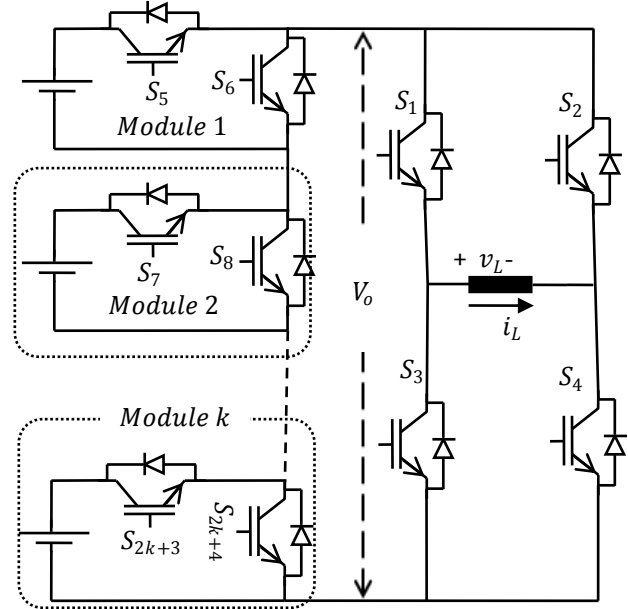


Fig 1. The proposed structure of multilevel inverter

Where,  $N_\alpha$  is the number of switching angles. In five-level inverter, for example, two switching angles with the condition  $\alpha_1 < \alpha_2 < \pi/2$  have been calculated. It is quite apparent that other angles can be obtained from these angles because of the quarter wave symmetry as shown in Fig. 2.  $S_5$  and  $S_7$  is the passkey of the five-level inverter. Therefore,  $\alpha_1$  and  $\alpha_2$  is calculated for these switches respectively. Switches' state, in the same module, cannot be simultaneously due to the fact that to elude short-circuit. In addition, H-bridge inverter's power switches  $S_1$  and  $S_4$  must be on conducting between  $\alpha_1$  and  $\pi - \alpha_1$  to get positive side of load voltage and in this section, current is positive. To get negative side of load voltage and make current negative,  $S_2$  and  $S_3$  are switched on between  $\pi + \alpha_1$  and  $2\pi - \alpha_1$ . In zero voltage step,  $S_1$  and  $S_2$  or  $S_3$  and  $S_4$  must be switched according to calculated switching time. Zero section's switching time changes based on phase angle between current and voltage.

In Fig. 2, the switching angles can be seen for one cycle of output voltage wave form. Dashed line in the figure represents the voltage (shown in Fig.1. as  $V_o$ ) applied to full-bridge and it's frequency is twofold of output voltage [1].

## III. DETERMINATION OF SWITCHING ANGLES

The control of multilevel inverter is based on specifying the switching angles to synthesize a desired sinusoidal voltage waveform.

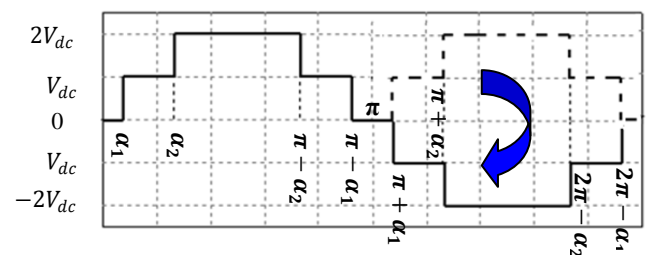


Fig 2. Output voltage wave form of 5-level inverter

In this paper, the stepped voltage waveform with odd-harmonic components is given in (8) for  $2k+1$  level inverter. Because of symmetric wave, output voltage has not included even-harmonic components. For equal dc sources, Fourier series expansion of the stepped output voltage is given with Eq. 8.

$$V_o(\omega t) = \sum_{n=1,3,\dots}^{\infty} \frac{4V_{dc}}{\pi n} [\cos(n\alpha_1) + \cos(n\alpha_2) + \dots + \cos(n\alpha_{k-1}) + \cos(n\alpha_k)] \sin \omega t \quad (8)$$

The desired effective value of output voltage,  $V_1$ , is controlled by using the modulation index and higher harmonic order desired to abolish have to been equal to zero. It is clear that so as to eliminate harmonic-order until the number of  $k-1$  and control modulation index, we need harmonic equations until the number of  $k$ . Therefore, for example, a nine-level inverter may ensure the control of modulation index and elimination of three harmonic-orders [8, 14].

The modulation index is given by:

$$M = \frac{V_1}{kV_{dc}} \quad (9)$$

Where,  $V_1$  is the first harmonic of the output voltage in the same time. For  $(2k+1)$  level inverter, harmonic equations until the number of  $k$  is given in the following equations first of which is related to desired output voltage value ( $V_1$ ).

Equation (10) changes according to harmonic-orders' number desired to eliminate and level number of multilevel inverter. These equations are transcendental and nonlinear. To handle this problem that consists of minimization the harmonics, optimization techniques are applied.

$$\begin{aligned} \cos(\alpha_1) + \cos(\alpha_2) + \dots + \cos(\alpha_{k-1}) + \cos(\alpha_k) &= Mk \frac{\pi}{4} \\ \cos(3\alpha_1) + \cos(3\alpha_2) + \dots + \cos(3\alpha_{k-1}) + \cos(3\alpha_k) &= 0 \\ &\vdots \\ \cos((N_{level} - 4)\alpha_1) + \dots + \cos((N_{level} - 4)\alpha_k) &= 0 \\ \cos((N_{level} - 2)\alpha_1) + \dots + \cos((N_{level} - 2)\alpha_k) &= 0 \end{aligned} \quad (10)$$

Conventional techniques such as Newton-Raphson method can be applied to this problem. But this method may not give optimum solution of equations above. Also, it is time consuming and complicated in accordance with GA. Therefore, in this paper the solution of the SHE equations has been solved by GA. This method uses fitness function to optimize the solution. In the solution of SHE problem, the fitness function must be THD's value given in (15)[1].

#### IV. GENETIC ALGORITHM BASED SHE TECHNIQUE

Genetic Algorithm is quantitative method that solves the problem and has been the most used technique to optimize a function which originates in constrained functions [12]. The algorithm solves the problem by using genetic operators, the types of which alter as to problem. And the algorithm can be adapted to an optimization problem easily. The flow-diagram of the algorithm is given in Fig. 3.

In order to solve SHE equations, the harmonic-orders desired to eliminate are depicted as constraint functions. After this state, it will be mentioned about the adaptation of SHE problem to GA for nine-level inverter. For example,

constraint functions are given in (11) for nine-level inverter eliminating 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup> harmonic components. GA evaluates these constraint functions and as a result, generates penalty functions. Thus, GA uses best population to optimize the problem. Population's size of each iteration is constant. But, chromosomes that constitute the population vary in accordance with evaluation of penalty function. Then crossover and mutation operators are applied. The all period is iterated as the number of iterations [16].

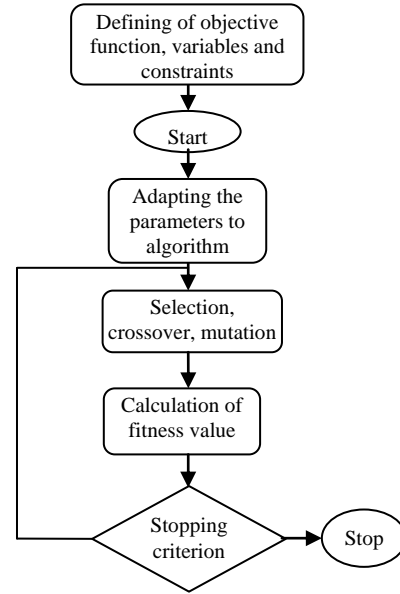


Fig 3. The flowchart of genetic algorithm

1., 2., 3. and 4. constraint functions are given respectively as:

$$\begin{aligned} \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) - Mk \frac{\pi}{4} &= 0 \\ \cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cos(3\alpha_4) &= 0 \\ \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) &= 0 \\ \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) &= 0 \end{aligned} \quad (11)$$

A basic GA can generate the chromosome including genes as binary coded or real coded. In this paper, real coded genetic algorithm has been used so as to solve SHE equations.

Algorithm is started numerically with producing of variables under the condition following equation;

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \pi/2 \quad (12)$$

The population changes according to type of problem, size of population is selected as 500.

Selection is reproduction of the starting population. In this paper, tournament selection is used. In tournament selection, two chromosomes are chosen randomly to become pairs. One of these pairs is specified according to the penalty function which is acquired from constraint function and incorporated in the new generation.

Penalty function evaluates closeness of the values of the chromosomes should be produced if there is any out of range of the constraint function. This range is between 0 and 0,01 in this study. This range determines precision of produced switching angles in multilevel inverter. The penalty function used in GA is given in following;

$$P(\alpha) = f(\alpha) + \sum_{k=1}^4 r[g_k(\alpha)] \quad (13)$$

where,  $P(\alpha)$  is penalty function,  $r=500$ ,  $g_k$  are constraint functions. The process of selection can be summarized with three sections;

- If both pairs of chromosomes are in appropriate range, that is constraint functions are not between 0 and 0,01, chromosome with small penalty function is incorporated in the new generation.
- If one of the pairs of chromosomes is in the appropriate range, that is the result of penalty function is equal to zero, this chromosome is incorporated in the new generations.
- If both pairs of chromosomes are in the appropriate range, chromosome with small fitness function is incorporated in the new generation.

One of the most notable parts of GA is crossover. Crossover performs creation of new offspring by taking into account selected chromosomes.

Several crossover techniques can be performed GA such as linear, arithmetic and heuristic etc. In this paper, arithmetical technique is used. In this technique, a number  $p$  which is named as crossover parameter is produced between 0 and 1 for each mutual gene of selected pairs of chromosomes. If this produced number is bigger than the cross rate, mutual genes are put into process of crossover as to arithmetically crossover equation (14). For example, if only 3<sup>rd</sup> genes are in the crossover for  $p=0,2$ , chromosomes are changed as in Table I and the arithmetically crossover equation is given by:

$$\begin{aligned} Gene_{3,CH1} &= pGene_{3,CH2} + (1-p)Gene_{3,CH1} \\ Gene_{3,CH2} &= pGene_{3,CH1} + (1-p)Gene_{3,CH2} \end{aligned} \quad (14)$$

TABLE I. ARITMETICALLY CROSSOVER SAMPLE OF GA SOLVING SHE EQUATIONS

Before crossover	Values of genes (rad)			
	Gene 1	Gene 2	Gene 3	Gene 4
Chromosome 1	0,21	0,44	0,8	1,4
Chromosome 2	0,36	0,77	0,91	1,36
After crossover	Values of genes (rad)			
	Gene 1	Gene 2	Gene 3	Gene 4
Chromosome 1	0,21	0,44	0,822	1,4
Chromosome 2	0,36	0,77	0,888	1,36

After crossover, mutation occurs. In real-coded GA, in order to perform mutation, a number is produced between 0 and 1 for each gene of each chromosome. If produced number for gene is lower than the mutation rate, gene is reproduced according to limits [15].

The most important point for the GA is evaluation of each chromosome. The aim of the study is to eliminate desired harmonic orders of output voltage in multilevel inverter, so fitness function must be associated to THD equation which may change based on harmonic orders and the number of harmonic orders desired to be equal zero [11]. For example, if the third, fifth, seventh harmonic orders are desired to

eliminate in nine-level inverter, fitness function is given by:

$$Fitness = \frac{\sqrt{\sum_{n=3,5,7} (\frac{1}{n} \sum_{k=1}^4 \cos(n\alpha_k))^2}}{\sum_{k=1}^4 \cos(\alpha_k)} \quad (15)$$

Consequently, the GA calculates the fitness function in each iteration and defines chromosomes as to fitness value. GA must select the chromosomes to minimization of desired harmonic orders. Therefore, the values of fitness functions should be equal to zero [1].

In this paper, elimination of 3<sup>rd</sup>, 7<sup>th</sup> harmonic order with 7-level output voltage has been aimed. In addition, with 9-level inverter 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup> harmonic order and 5<sup>th</sup>, 7<sup>th</sup>, 11<sup>th</sup> harmonic orders have been eliminated. In these harmonic elimination processes, modulation index is equal to 1. Finally, switching angles have been obtained by GA software including algorithm parameter in section IV. In Fig. 4, calculated switching angles can be seen for all harmonic elimination process.

## V. SIMULATION RESULTS

In this study, Selective Harmonic Elimination technique has been applied to seven-level and nine-level inverters. Simulation results have been given to assess the effectiveness of GA based SHE. The SHE equations were solved by GA and simulation was developed in Matlab&Simulink. The fundamental frequency of the output voltage is 50 Hz and switching frequency of the semiconductor power switches in the level module units and H-bridge is 100 Hz and 50 Hz, respectively.

TABLE II. SEVEN-LEVEL INVERTER % HARMONICS VALUE IN SPWM AND ELIMINATION OF 3<sup>rd</sup> AND 7<sup>th</sup> HARMONIC ORDERS IN SHEPWM AND SWITCHING ANGLES OF SHEPWM

Harmonic order	Amplitude of Harmonics %	
	SPWM	SHEPWM
		3 <sup>rd</sup> and 7 <sup>th</sup> harm. elimination
1	100	100
3	<b>1,5</b>	<b>0,16</b>
5	0,01	4,28
7	<b>2,25</b>	<b>0,17</b>
9	3,33	4,83
11	1,68	4,69

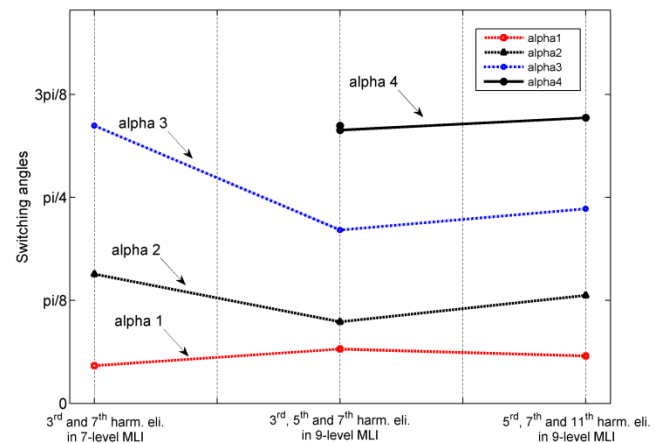


Fig 4. Switching angles calculated by GA for harmonic elimination in 7-level and 9-level inverter

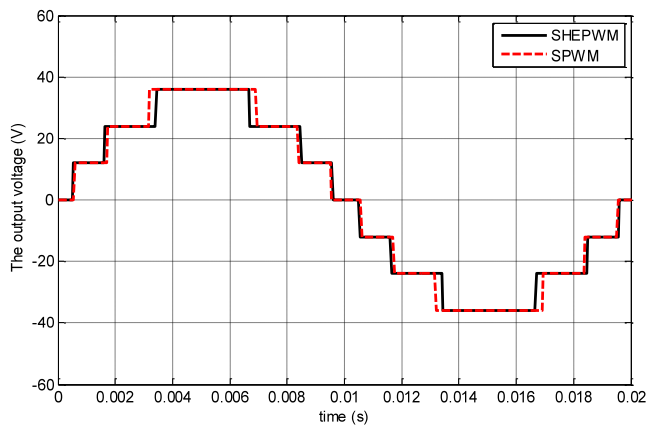


Fig 5. Output voltage waveforms in seven-level inverter with SPWM and SHEPWM eliminating 3<sup>rd</sup> and 7<sup>th</sup> harmonic orders

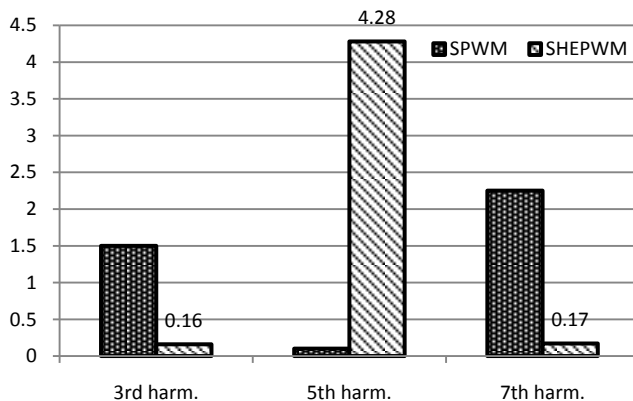


Fig 6. Elimination of 3<sup>rd</sup> and 7<sup>th</sup> harmonic orders in seven-level inverter

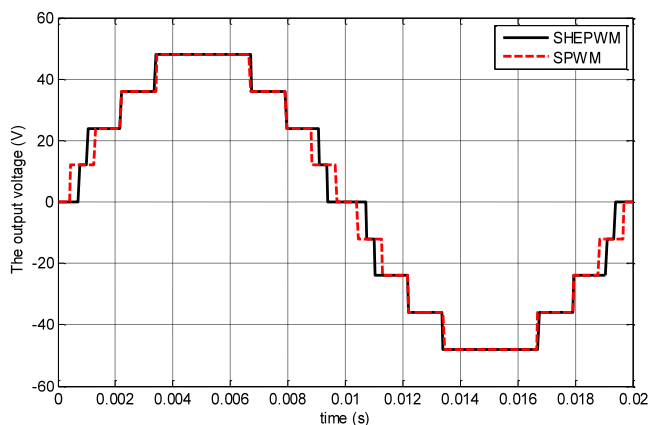


Fig 7. Output voltage waveforms in nine-level inverter with SPWM and SHEPWM eliminating 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonic orders

In Table II and Fig. 6, the eliminated harmonic orders are shown for seven-level inverter. Similarly, Table III and Fig. 8 give the results of nine-level inverter. Additionally, Fig. 5 shows the output voltage waveforms of seven-level inverter having 12 V isolated DC source. The output voltage's maximum rate is 36 V because of the three modules in seven-level inverter.

In Table II, it has been aimed at eliminate 3<sup>rd</sup> and 7<sup>th</sup> harmonic orders. While the eliminated harmonic orders are almost equal the zero, 5<sup>th</sup> harmonic component has increased from % 0,01 to % 4,28 when it is compared to SPWM. To overcome this, 5<sup>th</sup> harmonic component has been eliminated

TABLE III. NINE-LEVEL INVERTER % HARMONICS VALUE IN SPWM AND ELIMINATION OF 3<sup>RD</sup>, 7<sup>TH</sup>, 7<sup>TH</sup> HARMONIC ORDERS IN SHEPWM AND SWITCHING ANGLES OF SHEPWM

Harmonic order	Amplitude of Harmonics %	
	SPWM	SHEPWM
		3 <sup>rd</sup> , 5 <sup>th</sup> , 7 <sup>th</sup> harm. elimination
1	100	100
3	0,79	0,08
5	0,38	0,22
7	0,7	0,09
9	1,71	4,48
11	2,62	1,98

TABLE IV. NINE-LEVEL INVERTER % HARMONICS VALUE IN SPWM AND ELIMINATION OF 5<sup>TH</sup>, 7<sup>TH</sup>, 11<sup>TH</sup> HARMONIC ORDERS IN SHEPWM AND SWITCHING ANGLES OF SHEPWM

Harmonic order	Amplitude of Harmonics %	
	SPWM	SHEPWM
		5 <sup>th</sup> , 7 <sup>th</sup> , 11 <sup>th</sup> harm. elimination
1	100	100
3	0,79	4,71
5	0,38	0,14
7	0,7	0,12
9	1,71	3,2
11	2,62	0,1

in nine level inverter as shown in Table III and also in Fig. 8 clearly. In addition to this, Fig. 7 illustrates the output voltage waveforms of nine-level inverter. The output voltage's maximum rate is 48 V with four voltage step in positive side. The whole step consists of four voltage step in positive and four voltage step negative side and zero.

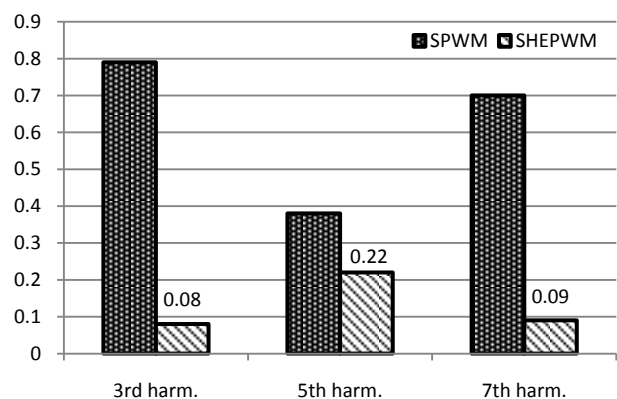


Fig 8. Elimination of 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonic orders in nine-level inverter

GA based SHE technique enables to eliminate any harmonic orders. To demonstrate this, 5<sup>th</sup>, 7<sup>th</sup>, 11<sup>th</sup> harmonic orders are eliminated in nine-level inverter. In Table IV and Fig. 9, the harmonic orders are shown for nine-level inverter. When compared Table III and Table IV, it is understood that with GA based SHE technique, harmonic orders desired to eliminate can be changed thanks to adaptability of SHE equations to any harmonic order. With the angles given in Table IV, three-phase simulation of the multilevel inverter, until 13<sup>th</sup> harmonics is eliminated because three-phase systems have no 3<sup>rd</sup>, 9<sup>th</sup>, 15<sup>th</sup>, .. etc. harmonic orders.



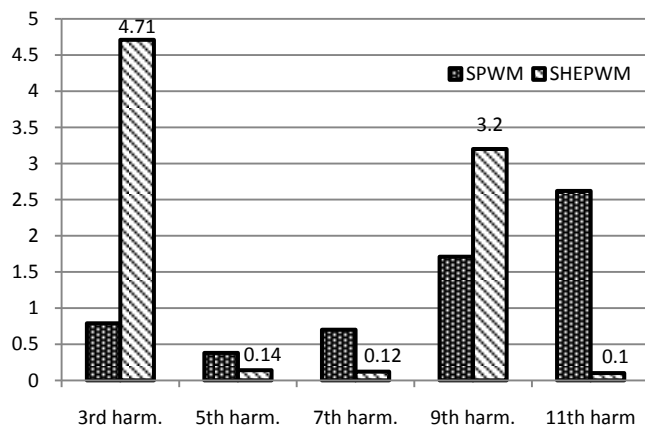


Fig 9. Elimination of 5<sup>th</sup>, 7<sup>th</sup> and 11<sup>th</sup> harmonic orders in nine-level inverter

## VI. CONCLUSION

GA based selective harmonic elimination in cascaded multilevel inverter with reduced number of switches has been presented. The advantage of proposed inverter topology is having a structure with the reduced number of switches. Therefore, the hardware cost of proposed multilevel inverter is lower than multilevel inverter with H-bridge modules and it is compact. Also, switching techniques applied to conventional multilevel inverter can be used with this topology.

SHE equations of the output voltage of seven-level and nine-level multilevel inverter have been solved by the developed GA software without the use of GA toolbox of MATLAB and applied to the proposed inverter topology. The obtained results have clearly proved the effectiveness of the proposed multilevel structure and GA based SHE method.

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