Active Tunable Lossy Inductance Simulation Using Single Fully Balanced Voltage Differencing Buffered Amplifier

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***Abstract*—Two active configurations for simulating tunable floating and grounded lossy inductors are described. Each simulated inductor circuit contains only a single fully balanced-voltage differencing buffered amplifier (FB-VDBA), one resistor, and one capacitor. The equivalent values of the simulated elements can be tuned independently through the FB-VDBA's bias current and/or the resistor in the circuit. Non-ideal analysis of the synthetic inductors is also provided. The practical use of the proposed FB-VDBA based lossy inductance simulators is demonstrated on both a second-order RLC low-pass filter and a parallel RLC resonance circuit. PSPICE simulation results are provided to evaluate the presented theory.**

***Index Terms*—Fully Balanced-Voltage Differencing Buffered Amplifier (FB-VDBA), RL impedance simulator, lossy inductor, inductance simulation**

I. Introduction

An active simulation of lossy inductors has become a fascinating research topic for electrical engineers, circuit researchers, and scientists, since it is useful in active network synthesis, and microelectronic applications, such as active filters, LC oscillators, and impedance matching and parasitic cancellation circuitry. From the viewpoint of the advent of integrated circuit (IC) technology, the design of synthetic active inductances can be applied instead of the bulky discrete inductors in passive circuits. Accordingly, several active circuits for synthetic lossy inductance simulation have been developed earlier using various types of active elements [1]-[31]. These inductance simulators can usually be classified as floating [1]-[13] and grounded [14]-[31] configurations. It can be observed in [1]-[5], [7], [9], [11]-[13], [19], [21], [23] that the realizations are composed of more than one active components. Some of them also use three or more grounded and/or floating passive components [1]-[5], [9], [11], [19], [21], [23], [31]. Moreover, in [2]-[3], [5], [9], [12], any kind of critical element-matching and/or cancellation constraints are necessarily required. A topology without such matching requirements is considered to be a favorable feature for the desired realization. Apart from that, the methods in [6], [8], [10], [14]-[18], [20], [22], [24]-[30] utilize a single active component to simulate floating and grounded lossy inductors. However, the designs still need an excessive number of passive elements, i.e. at least three passive elements, and do not provide electronic control facility. In addition to [8], [14]-[15], [25]-[27], there are requirements for any certain component-matching or cancellation conditions.

The main objective of this work is, therefore, to introduce two tunable lossy inductance simulator circuits, which realize floating series RL impedance and grounded parallel RL impedance. The introduced lossy simulated inductors both employ only one fully balanced-voltage differencing buffered amplifier (FB-VDBA) [32]-[36] as well as a low number of passive elements, namely one resistor and one capacitor. The simulated inductor circuits are devoid of any certain component-matching or cancellation constraints. The simulated resistance and inductance elements of the circuits in both cases can be varied electronically by the transconductance gain of the FB-VDBA. The effects of the transfer error and parasitic elements of the FB-VDBA on the resulting inductor structures are also examined. The presented theory has been verified by simulation results based on CMOS TSMC 0.25-μm process parameters. A detailed comparison of the proposed inductance simulators with the previously similar solutions [1]-[31] is presented in Table I.

II. Fully Balanced-Voltage Differencing Buffered Amplifier (FB-VDBA)

The symbolic representation of the ideal FB-VDBA device is shown in Fig.1, which can be characterized by the following matrix equation [33]-[35].

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TABLE I
PHYSICAL COMPARISON OF THE PROPOSED INDUCTANCE SIMULATORS WITH SOME EARLIER WORKS.

Ref.	Inductor terminal	Inductor type	No. of active element	No. of passive element	Matching requirement	Availability of electronic tuning	Supply voltages
[1]	Floating	series (Fig.1b)	CCII = 2	R = 2, C = 1	no	no	NA
		parallel (Fig.1c)					
[2]		series (Fig.2b)	OA = 2, OTA = 1	R = 2, C = 1	yes	no	NA
		parallel (Fig.2c)					
[3]		series, (Fig.3f)	OA = 2	R = 3, C = 2	yes	no	NA
		parallel (Fig.3c)	OA = 1, OTA = 1	R = 3, C = 1	no	yes	
[4]		series, (Fig.3a, 3c, 3f, 3g)	CCII = 2	R = 2, C = 1	no	no	NA
		parallel, (Fig.3b, 3d, 3e, 3h)					
[5]		parallel	CCII = 2	R = 2, C = 1	yes	no	±12V
[6]		series	CCII = 1	R = 2, C = 1	no	no	NA
[7]		series, (Fig.3)	CCCII+ = 2, CCCII- = 1	C= 1	no	yes	±2.5V (simulation), ±5V (experiment)
		parallel (Fig.2)	CCCII- = 2				
[8]		series/parallel	DDCC = 1	R = 2, C = 1	no	no	±0.9V, -0.34V
[9]		parallel	CFOA = 2	R = 3, C = 2	yes	no	±15V
[10]		parallel, (Fig.2)	DO-DDCC = 1	R = 2, C = 1	no	no	±1.5V, -0.9V
[11]		series, (Fig.1a)	CFOA = 2	R = 2, C = 1	no	no	NA
		parallel (Fig.1b)					
[12]		series, (Fig.2)	VDBA = 2	R = 1, C = 1	yes	yes	±0.75V (simulation), ±5V (experiment)
		parallel (Fig.3)					
[13]		series	FB-VDBA = 2	C = 1	no	yes	±1V
[14]	Grounded	series	CCII = 1	R = 3, C = 4	yes	no	NA
[15]		series	CFOA = 1	R = 3, C = 1	yes	no	NA
[16]		series	FTFN = 1	R = 2, C = 1	no	no	NA
		parallel					
[17]		parallel, (Fig.1)	CCII = 1	R = 2, C = 1	no	no	NA
		parallel, (Fig.2)	CCI = 1, CCIII = 1	R = 1, C = 2	no	no	NA
[18]		series/parallel	CCIII = 1	R = 2, C = 1	no	no	±2.5V
[19]		parallel	CCII = 3	R = 3, C = 3	no	no	±12V
[20]		parallel, (Fig.2a)	OTRA = 1	R = 2, C = 1	no	no	±5V
[21]		parallel, (Fig.2a)	OTRA = 2	R = 4, C = 1	no	no	±10V
[22]		series, (Fig.2a)	DVCC = 1	R = 2, C = 1	no	no	±2.5V
		parallel, (Fig.3a)					
[23]		parallel	VF = 2, CF = 1	R = 3, C = 1	no	no	±1.25V, 0.4V
[24]		parallel	CDBA = 1	R = 2, C = 1	no	no	±12V
[25]		parallel	CCIII = 1	R = 3, C = 1	no	no	±10V
[26]		parallel	DXCCII = 1	R = 2, C = 1	yes	no	±1.5V
[27]		series/parallel	DXCCII = 1	R = 3, C = 1	yes	no	±2.5V, 1.44V
[28]		series	CFOA = 1	R = 2, C = 1	no	no	±10V
[29]		series	VDCC = 1	R = 1, C = 1	no	no	±0.9V
[30]		series/parallel	CFOA = 1	R = 2, C = 1	no	no	±0.75V, 0.34V
[31]		series	VDBA = 1	R = 1, C = 1	no	no	±0.75V
Proposed circuits	Floating	series	FB-VDBA	R = 1, C = 1	no	yes	±0.75V
	Grounded	parallel					

NA : Not Available
CCI : first-generation current conveyor, CCII : second-generation current conveyor, CCIII : third-generation current conveyor, CCCII± : positive/negative current-controlled conveyor, DDCC : differential difference current conveyor, DO-DDCC : dual-output differential difference current conveyor, DVCC : differential voltage current conveyor, DXCCII : dual-X current conveyor, VDCC : voltage differencing current conveyor, OA : operational amplifier, OTA : operational transconductance amplifier, CFOA : current feedback operational amplifier, OTRA : operational transresistance amplifier, VDBA : voltage differencing buffered amplifier, FTFN : four-terminal floating nullor, CDBA : current differencing buffered amplifier, VF : voltage follower, CF : current follower,

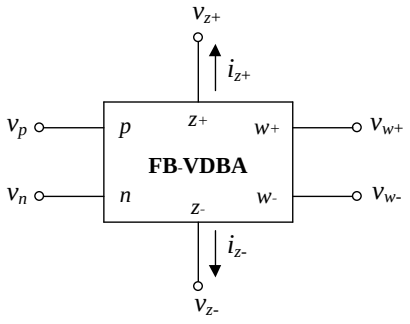


Fig. 1. Electrical circuit symbol of the FB-VDBA.

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ v_{w+} \\ v_{w-} \end{bmatrix} = \begin{bmatrix} \alpha_p g_m & -\alpha_n g_m & 0 & 0 \\ -\alpha_p g_m & \alpha_n g_m & 0 & 0 \\ 0 & 0 & \beta_p & 0 \\ 0 & 0 & 0 & \beta_n \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_{z+} \\ v_{z-} \end{bmatrix} \quad (1)$$

In (1), g_m is the small-signal transconductance gain of the FB-VDBA, which is scaled electronically by electronic means. Also, the parameters α_i and β_i (i = p, n) are respectively the non-ideal transconductance gains and the

non-ideal voltage gains, which are equal to unity in the ideal case. The possible structure realization of the FB-VDBA is given in Fig.2, where its internal part is functionally a connection of dual-out operational transconductance amplifier (OTA) M_1-M_{12} and two voltage buffers M_{13}-M_{16} and M_{17}-M_{20} [33]-[35]. Therefore, this device utilizes features of tunable OTA and voltage follower in a single integrated circuit structure. The FB-VDBA transconductance gain, which is realized in the OTA stage, is determined by the following relation.

$$g_m = \sqrt{KI_B} \tag{2}$$

where $K = \mu_0 C_{ox} W/L$ is the MOS transistor transconductance, W and L are the channel width and length, respectively, μ_0 is the carrier and C_{ox} is the gate-oxide capacitance per unit area. In this design, the transistor dimensions (W/L) of the FB-VDBA realization in Fig.2 are given in Table II.

TABLE II
GEOMETRICAL ASPECT RATIOS (W/L) OF TRANSISTORS IN FIG.2.

Transistors	W/L (μm/μm)
$M_1 - M_2$	8/0.25
M_3 , M_6	12/0.25
$M_4 - M_5$, $M_7 - M_{12}$	20/0.25
$M_{13} - M_{20}$	60/0.25

III. PROPOSED LOSSY INDUCTANCE SIMULATOR CIRCUITS

The proposed circuits for realizing floating and grounded lossy inductors are shown in Fig.3 and 4, respectively. Both of the circuits are implemented with a single FB-VDBA, one resistor, and one capacitor. For the ideal case, i.e. $\alpha_i = \beta_i = 1$, the input impedance and admittance functions of the proposed inductance simulators in Fig.3 and 4 are respectively obtained as follows:

$$Z_{in1} = \frac{v_{in1}}{i_{in1}} = R_{eq1} + sL_{eq1} = \frac{1}{g_m} + s\left(\frac{R_1 C_1}{g_m}\right), \tag{3}$$

and

$$Y_{in2} = \frac{i_{in2}}{v_{in2}} = \frac{1}{R_{eq2}} + \frac{1}{sL_{eq2}} = \frac{1}{R_2} + \frac{g_m}{sR_2 C_2}. \tag{4}$$

From these results, it follows that the proposed circuit of Fig.3 simulates a floating lossy series RL-type inductor with equivalent resistance $R_{eq1} = 1/g_m$ and equivalent inductance $L_{eq1} = R_1 C_1/g_m$, and the proposed circuit of Fig.4 realizes a grounded parallel RL impedance with $R_{eq2} = R_2$ and $L_{eq2} = R_2 C_2/g_m$. It is further observed that in both circuits the simulated inductance value is adjustable independently via R_1 and/or C_1 in the circuit of Fig.3, and via g_m and/or C_2 in the circuit of Fig.4. Two proposed circuits are also free from any passive component-matching constraints for inductance simulations.

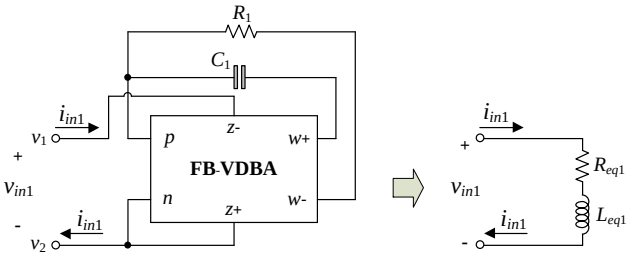


Fig. 3. Proposed floating lossy series-type inductance simulation and its equivalent model.

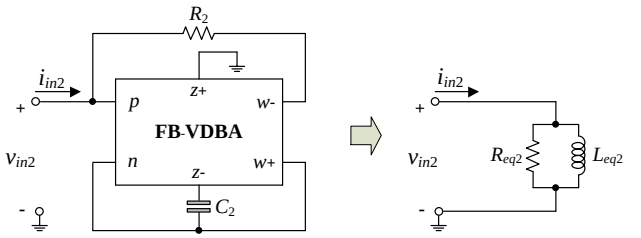


Fig. 4. Proposed grounded lossy parallel-type inductance simulation and its equivalent model.

IV. EFFECT OF TRANSFER ERRORS

Considering the non-ideal parameters α_i and β_i gave in (1), the one-point impedance function looking into terminal 1 for the simulator circuit in Fig.3 can be found as:

$$Z'_{in1}\big|_{v_2=0} = \frac{v_1}{i_{in1}} = R'_{eq1} + sL'_{eq1} = \left(\frac{1}{\alpha_n g_m}\right) + s\left(\frac{R_1 C_1}{g_m}\right)\left(\frac{\beta_p}{\alpha_n \beta_n}\right). \tag{5}$$

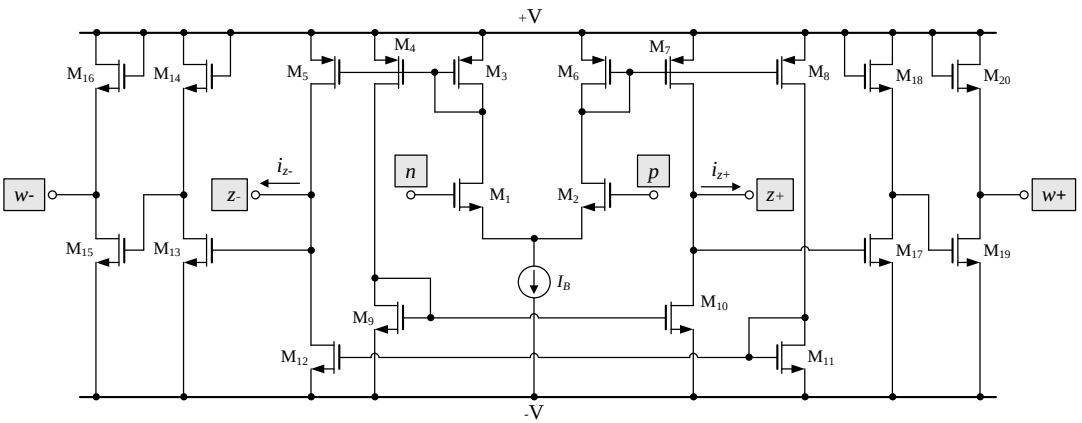


Fig. 2. Circuit diagram of the CMOS FB-VDBA.

On the other hand, the one-point impedance function looking into terminal 2 of Fig.3 can be written as:

$$Z''_{in1}\big|_{v_1=0} = -\frac{v_2}{i_{in1}} = R''_{eq1} + sL''_{eq1} = \left(\frac{1}{\alpha_p g_m}\right) + s\left(\frac{R_1 C_1}{g_m}\right)\left(\frac{\beta_p}{\alpha_p}\right). \quad (6)$$

In the same way, the α_i and β_i gains are also taken into consideration to evaluate the performance of the second developed lossy parallel-type inductance simulator of Fig.4. Therefore, considering non-idealities into account, the input admittance from (4) modifies as:

$$Y'_{in2} = \frac{i_{in2}}{v_{in2}} = \frac{1}{R'_{eq2}} + \frac{1}{sL'_{eq2}} = \frac{1}{R_2} + \left(\frac{g_m \alpha_n \beta_n}{sR_2 C_2}\right). \quad (7)$$

It readily shows in (5)-(7) that the non-ideal transfer gains of FB-VDBA affect the input equivalent impedances of the proposed circuits, and as a result lesser the α_i and β_i non-ideal gains, the lesser is the influence on the simulator. It is also noted that the proper tuning of the g_m-value may practically lead to the reduction of the non-ideal transfer gain effect.

V. Effect of Parasitic Impedances

Consider the non-ideal behavior model of the FB-VDBA shown in Fig.5. The shunt parasitic impedances (R//C) appear at terminals p, n, z+, and z-, respectively, whereas the resistances R_{w+} and R_{w-} are the serial parasitic resistances at terminals w+ and w-. Using the non-ideal model of the FB-VDBA in presence of parasitic impedances, the proposed inductance simulator circuits in Fig.3 and 4 can be redrawn as represented in Fig.6 and 7, respectively. Thus, taking into account the FB-VDBA parasitics outlined above and reanalyzing the real behavior of the proposed floating lossy inductance simulator in Fig.6, the non-ideal input impedance becomes:

$$Z_{in1} = \left[\frac{1}{g_m(1+sR_{w+}C_1)}\right] + \left[\frac{s(R_1 + R_{w+} + R_{w-})C_1}{g_m(1+sR_{w+}C_1)}\right]. \quad (8)$$

Assumed that in practice the above relation is $R_1 >> R_{w+}$, R_{w-}, then the impedance Z_{in1} can be approximated to

$$Z_{in1} = Z_1 + Z_2 \cong \left[\frac{1}{g_m(1+sR_{w+}C_1)}\right] + \left[\frac{sR_1C_1}{g_m(1+sR_{w+}C_1)}\right], \quad (9)$$

where $$Y_1 = \frac{1}{Z_1} = g_m + s(g_m R_{w+} C_1) = \frac{1}{R^*_{eq1}} + sC_{ext1}, \quad (10)$$

and $$Y_2 = \frac{1}{Z_2} = \left[\frac{g_m}{sR_1C_1}\right] + \left[\frac{g_m R_{w+} C_1}{R_1}\right] = \frac{1}{sL^*_{eq1}} + \frac{1}{R_{ext1}}. \quad (11)$$

From (9)-(11), it is important to note that an extra intrinsic capacitance C_{ext1} appears in shunt with the parasitic resistance R^*_{eq1}. It may be also mentioned that in the same branch an extra intrinsic resistance R_{ext1} is also in parallel with the parasitic inductance L^*_{eq1}. Thus, if the FB-VDBA parasitic impedances are included, an equivalent circuit of the proposed floating lossy inductance simulator in Fig.3 is redrawn in Fig.8. However, if the condition $R_{w+} << 1/g_m$, R_1 is satisfied, then the parasitic effects of the FB-VDBA are reduced.

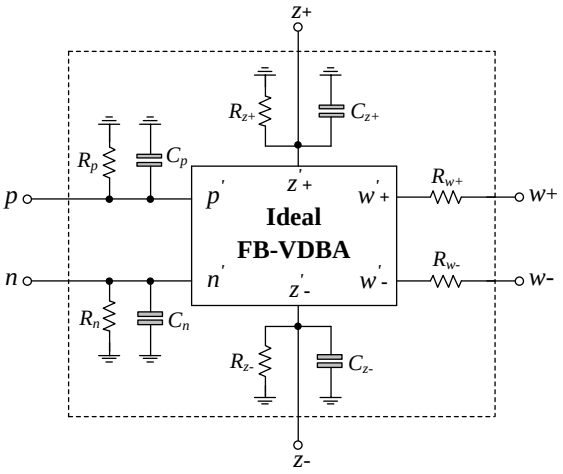


Fig. 5. Non-ideal model of the FB-VDBA with parasitic elements.

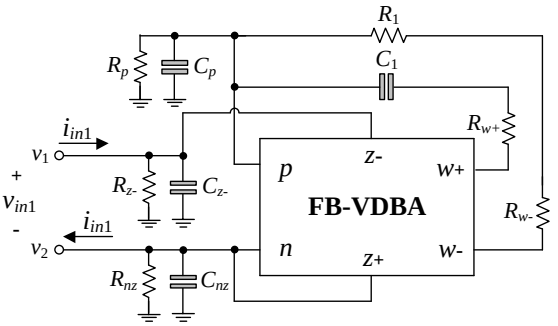


Fig. 6. Proposed floating lossy inductance simulator of Fig.3 including parasitic elements.

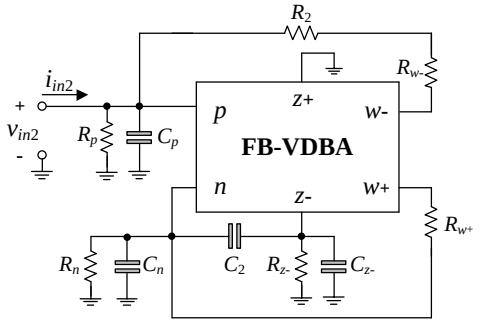


Fig. 7. Proposed grounded lossy inductance simulator of Fig.4 including parasitic elements.

Similarly, for the proposed grounded lossy inductor in Fig.7, the input admittance for the common case of $C_2 >> C_n$, C_{z-} and $R_{z-} >> R_{w+}$ is found approximately as:

$$Y_{in2} = Y_A + Y_B \cong \left[\frac{sR_{z-}C_2(1+g_m R_{w+})}{(R_2+R_{w-})(1+sR_{z-}C_2)}\right] + \left[\frac{g_m R_{z-}}{(R_2+R_{w-})(1+sR_{z-}C_2)}\right], \quad (12)$$

where

$$Z_A = \frac{1}{Y_A} = \left(\frac{R_2+R_{w-}}{1+g_m R_{w+}}\right) + \left[\frac{R_2+R_{w-}}{sR_{z-}(1+g_m R_{w+})C_2}\right] = R^*_{eq2} + \frac{1}{sC_{ext2}}, \quad (13)$$

and

$$Z_B = \frac{1}{Y_B} = s\left[\frac{(R_2 + R_{w-})C_2}{g_m}\right] + \left(\frac{R_2 + R_{w-}}{g_m R_{z-}}\right) = sL^*_{eq2} + R_{ext2}. \quad (14)$$

From (12)-(14), an equivalent circuit including FB-VDBA parasitic impedances for the proposed inductance simulator circuit in Fig.4 can be represented in Fig.9. One observes from above mentioned mathematical results that $R_2 >> R_{w-}$ must be satisfied to prevent the parasitic effects on R^*_{eq2} and L^*_{eq2}. It also follows from (13) and (14) that if the value of parasitic resistance R_{z-} is high enough, the extra impedances (R_{ext2} and C_{ext2}) do not affect the impedance of the inductor.

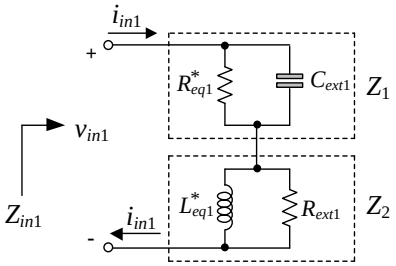


Fig. 8. Non-ideal equivalent model of the proposed floating lossy inductance simulator in Fig.3 including parasitic impedances.

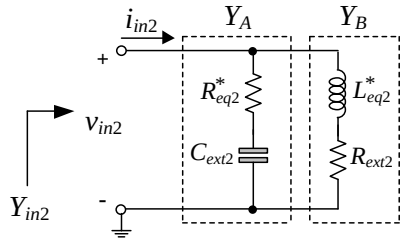


Fig. 9. Non-ideal equivalent model of the proposed grounded lossy inductance simulator in Fig.4 including parasitic impedances.

VI. Simulations and Functional Verifications

To verify the functionality of the proposed lossy inductance simulator circuits, PSPICE simulations were carried out based on a standard 0.25-μm CMOS process parameters from TSMC [37]. The proposed circuits in Fig.3 and 4 are simulated by using the FB-VDBA in Fig.2 with power supply voltages fixed at ±0.75 V.

A. Simulation results of the proposed floating lossy inductance simulator circuit in Fig.3

The simulated transient responses of the proposed circuit in Fig.3 are represented in Fig.10 with g_m = 0.5 mA/V ($I_B \cong$ 30 μA), R_1 = 1 kΩ and C_1 = 0.1 nF. Using (3), the simulated equivalent elements are obtained as R_{eq1} = 2 kΩ and L_{eq1} = 0.2 mH. In Fig.10, it is found that the phase shift between v_{in1} and i_{in1} is about 31° when the sinusoidal input signal of an amplitude 80 mV (peak) at 1 MHz was applied to the circuit. On the other hand, the simulation and ideal frequency characteristics of the impedance Z_{in1} are also plotted in Fig.11. The simulated responses agree well quite with the theoretical results, which confirm the proper operation of the proposed circuit. In addition to simulation results, the total power consumption of the circuit in Fig.3 was found as 14.1 mW.

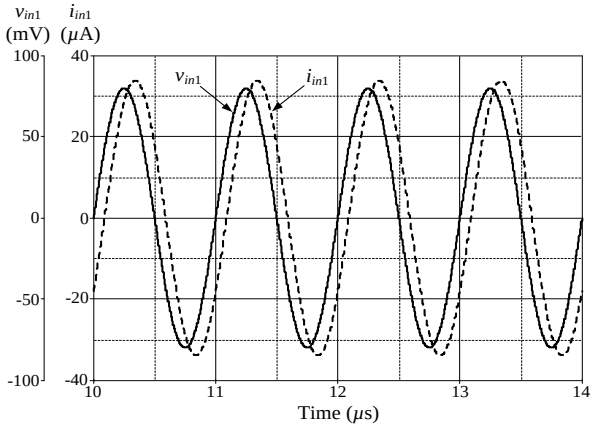


Fig. 10. Simulated transient responses for v_{in1} and i_{in1} of the proposed floating lossy inductance simulator in Fig.3.

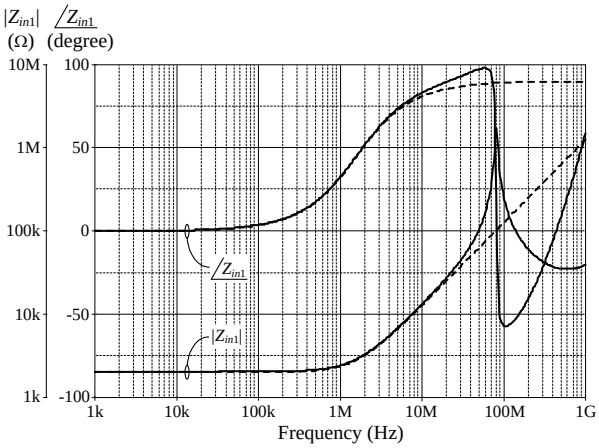


Fig. 11. Theoretical (dashed lines) and simulation (solid lines) magnitude and phase responses of Z_{in1} of Fig.3.

Fig.12 shows the simulated magnitude responses of Z_{in1} with R_{eq1} tuning while keeping L_{eq1} constant. This design is for L_{eq1} = 0.2 mH with C_1 = 0.1 nF, and simultaneously changing the values of g_m and R_1 as follows: (0.25 mA/V and 0.5 kΩ), (0.50 mA/V and 1 kΩ), (0.75 mA/V and 1.5 kΩ), (1 mA/V and 2 kΩ), and (1.25 mA/V and 2.5 kΩ), which results in R_{eq1} = 4 kΩ, 2 kΩ, 1.34 kΩ, 1 kΩ, and 0.8 kΩ, respectively. Fig.13 also shows the Z_{in1}-magnitude frequency variation concerning R_1-value (i.e., 2.5 kΩ, 2 kΩ, 1.5 kΩ, 1 kΩ, and 0.5 kΩ). The values of g_m = 0.5 mA/V and C_1 = 0.1 nF are taken to obtain R_{eq1} = 2 kΩ for all plots. For a given R_1, the corresponding L_{eq1} values are simulated as 0.5 mH, 0.4 mH, 0.3 mH, 0.2 mH, and 0.1 mH, respectively.

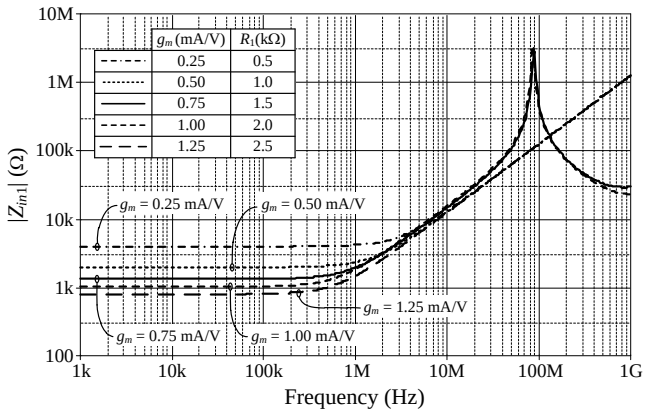


Fig. 12. Simulated Z_{in1}-magnitude responses with tuning R_{eq1}.

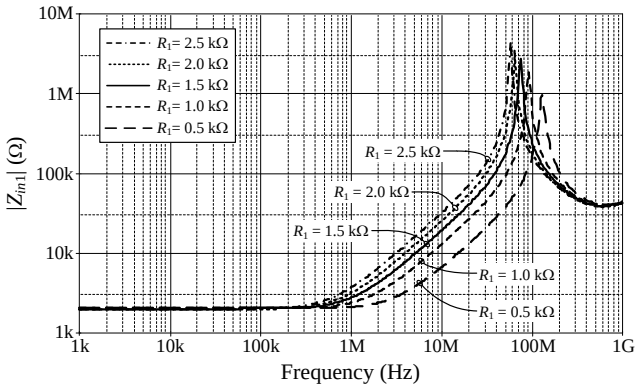


Fig. 13. Simulated Z_{in1}-magnitude responses with tuning L_{eq1}.

B. Simulation results of the proposed grounded lossy inductance simulator circuit in Fig.4

For the proposed grounded lossy parallel-type inductance simulator circuit of Fig.4, the time-domain and frequency responses for g_m = 0.5 mA/V, R_2 = 1 kΩ and C_2 = 0.1 nF are shown in Fig.14 and 15, respectively. According to (4), the simulated equivalent elements can be realized as R_{eq2} = 1 kΩ and L_{eq2} = 0.2 mH. As can be observed from Fig.14, when an input sine-wave signal with 1 MHz and amplitude of 80 mV has been applied, its phase difference is around 38°. In this case, the total power dissipation of the simulated lossy inductor is about 15.3 mW for a given bias condition.

It may also be observed from (4) that the R_{eq2} variation can be accomplished by the adjustment of R_2. Moreover, the R_{eq2} tuning can be obtained without affecting L_{eq2} by keeping the R_2/g_m ratio constant. The orthogonal adjustment of R_{eq2} and L_{eq2} is demonstrated in Fig.16 by plotting the Z_{in2}-magnitude responses for R_{eq2} = R_2 = 1 kΩ, 1.5 kΩ, 2 kΩ and 2.5 kΩ, while keeping R_2/g_m fixed at 2×10^{-6}. On the other hand, the simulated magnitude responses of Z_{in2} are depicted in Fig.17 for L_{eq2} = 0.3 mH, 0.4 mH, 0.5 mH and 0.7 mH, when R_{eq2} remains constant at 2 kΩ. It is evident from both figures that the simulated equivalent elements R_{eq2} and L_{eq2} can be tuned orthogonally.

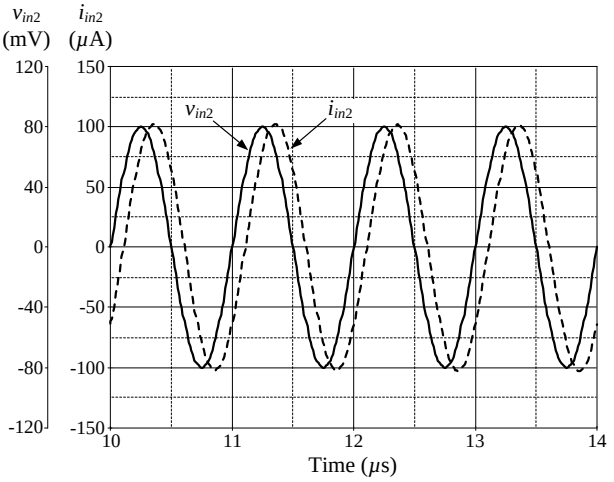


Fig. 14. Simulated transient responses for v_{in2} and i_{in2} of the proposed grounded lossy inductance simulator in Fig.4.

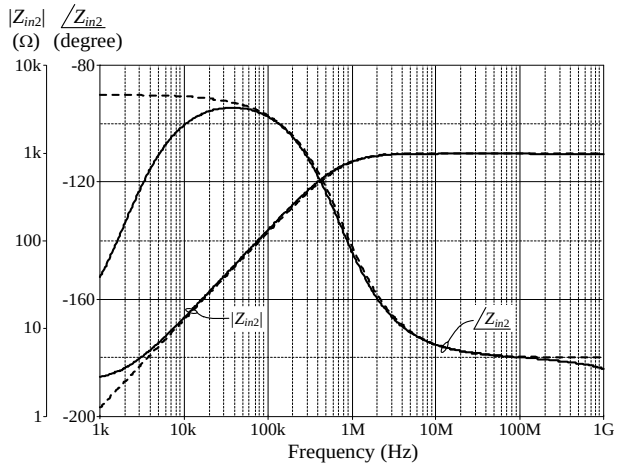


Fig. 15. Theoretical (dashed lines) and simulation (solid lines) magnitude and phase responses of Z_{in2} of Fig.4.

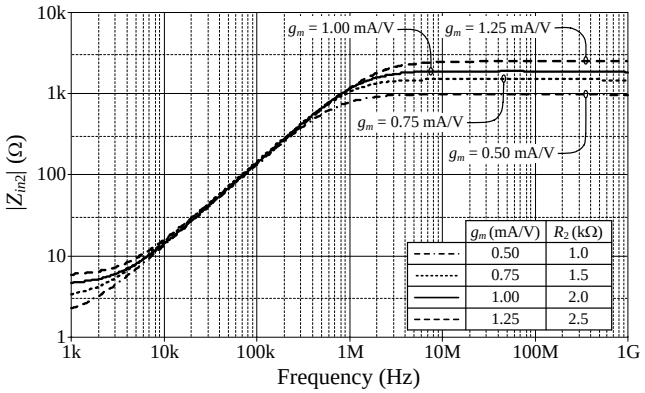


Fig. 16. Simulated Z_{in2}-magnitude responses with tuning R_{eq2}.

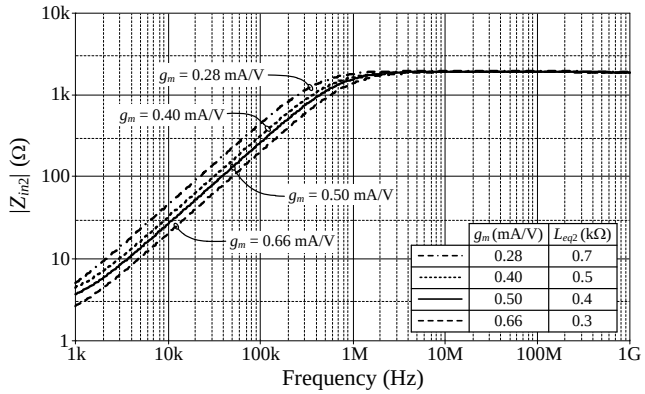


Fig. 17. Simulated Z_{in2}-magnitude responses with tuning L_{eq2}.

VII. Application Examples

As the first application of the proposed floating inductance simulator circuit in Fig.3, it was employed to implement a second-order RLC low-pass filter [38], as shown in Fig.18. Routine analysis of the configuration of Fig.18 shows that the voltage transfer function, the pole frequency (f_p), and the quality factor (Q) are found as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\left(\frac{g_m}{R_1C_1C_{LP}}\right)}{s^2 + \left(\frac{s}{R_1C_1}\right) + \left(\frac{g_m}{R_1C_1C_{LP}}\right)}, \qquad (15)$$

$$\omega_p = 2\pi f_p = \sqrt{\frac{g_m}{R_1 C_1 C_{LP}}}, \tag{16}$$

and

$$Q = \sqrt{\frac{g_m R_1 C_1}{C_{LP}}}. \tag{17}$$

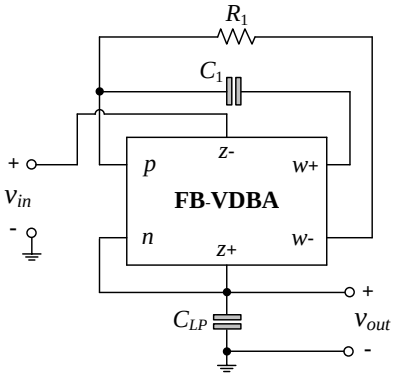
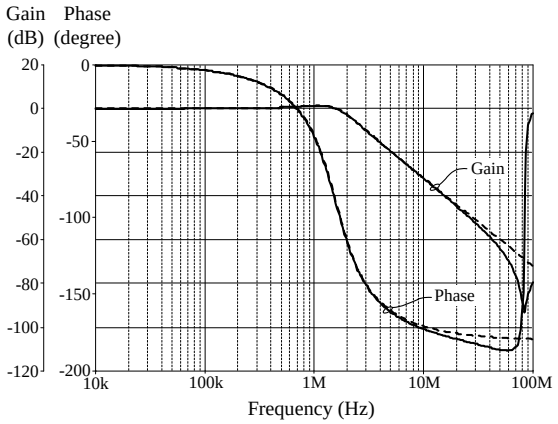
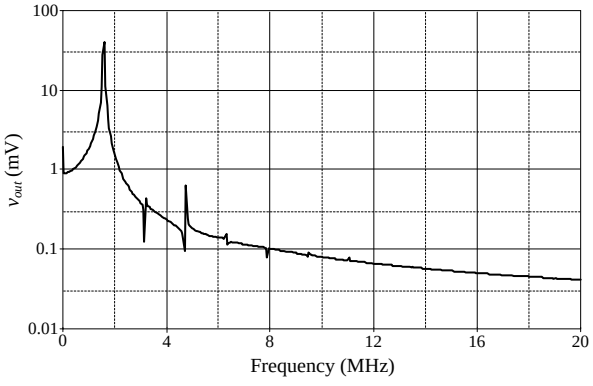


Fig. 18. Second-order RLC low-pass filter using the proposed floating inductance simulator circuit in Fig.3.

The circuit components for the realization are chosen as g_m = 0.5 mA/V, R_1 = 1 kΩ, C_1 = 0.1 nF and C_{LP} = 50 pF, corresponding to the important filter characteristics as: f_p = 1.58 MHz and Q = 1. The frequency characteristics of the resulting low-pass filter are depicted in Fig.19. The value of the corresponding f_p measured from the simulation is 1.60 MHz, which demonstrates a close agreement with the theoretical value.



(a)



(b)

Fig. 19. Frequency characteristics of the low-pass filter in Fig.18.
(a) gain and phase frequency characteristics (theoretical--dashed lines, simulation--solid lines) (b) frequency spectrum.

The electronic tunability of the realized low-pass filter can be assessed by changing the transconductance g_m of the FB-VDBA. The gain-frequency domain behavior with respect to g_m (i.e., g_m = 0.2 mA/V, 0.3 mA/V, 0.5 mA/V, and 1 mA/V) is shown in Fig.20. As mentioned in (16) and (17), the ideal pole frequencies are f_p = 1 MHz, 1.3 MHz, 1.58 MHz, and 2.25 MHz, and the ideal quality factors are Q = 0.65, 0.82, 1, and 1.41. The total harmonic distortion variations (THD) variation in the filter output is also measured by applying sinusoidal input voltages at 1.58 MHz. The obtained results are plotted in Fig.21, which is observed that the THD remains below 10% for input voltage signal up to 300 mV.

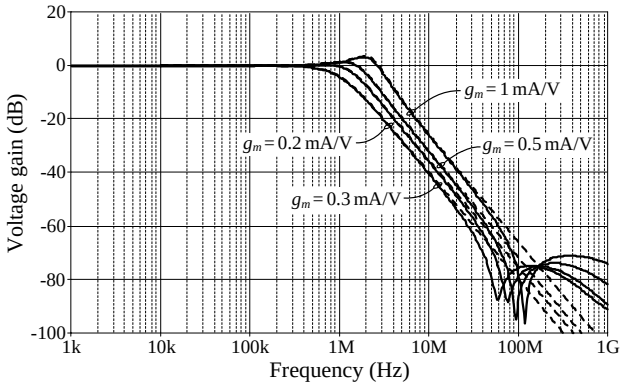


Fig. 20. Simulated gain-frequency responses of the low-pass filter in Fig.18 with respect to g_m.

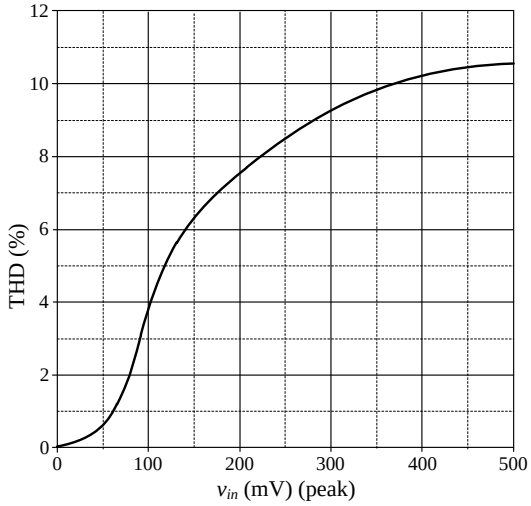


Fig. 21. THD variations of the filter in Fig.18 against the input signal amplitude.

Furthermore, the RLC parallel resonance circuit in Fig.22 is performed to verify the functionality of the proposed grounded inductance simulator circuit of Fig.4. For this purpose, the parallel R and L in the prototype passive circuit is replaced by the simulated parallel RL of Fig.4. The component values are taken as R_2 = 2 kΩ, C_2 = 0.1 nF and C_{RES} = 50 pF, to achieve R_{eq2} = 2 kΩ. The simulated plots of the magnitude-frequency characteristic at different g_m values (i.e. 0.28 mA/V, 0.40 mA/V, 0.66 mA/V, and 1 mA/V) are given in Fig.23. This adjustment results in different L_{eq2} values, i.e. 0.7 mH, 0.5 mH, 0.3 mH and 0.2 mH, respectively.

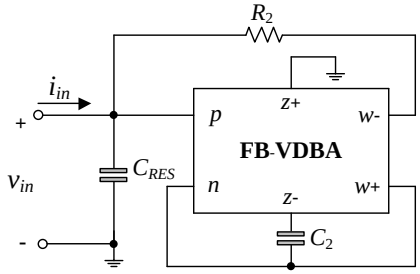


Fig. 22. RLC parallel resonance circuit using the proposed grounded inductance simulator circuit in Fig.4.

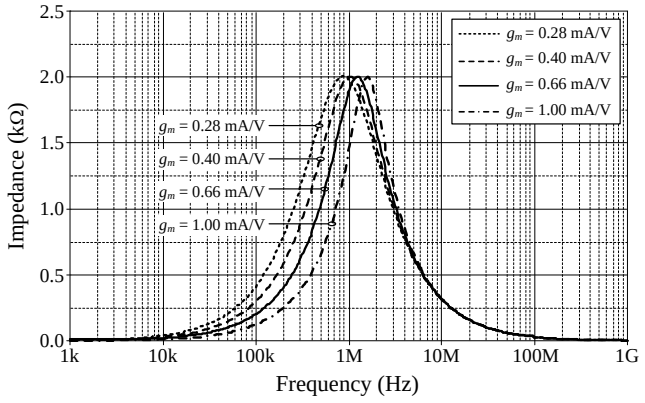


Fig. 23. Magnitude-frequency plots of the RLC resonance circuit for different g_m values.

VIII. Conclusions

In this article, series and parallel lossy inductance simulating configurations using a fully balanced voltage differencing buffered amplifier (FB-VDBA) are presented Each present topology utilizes only one FB-VDBA, one resistor, and one capacitor. The tuning of the simulated equivalent elements is realized by adjusting the bias current and/or the resistor in the simulators. As application examples, RLC second-order low-pass filter and parallel resonance circuits are constructed using the proposed lossy inductance simulators. Simulation results are given to verify the functionality of the proposed inductor circuits.

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