Design of the Adaptive Impedance Buffer in Low Quiescent Current LDO

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***Abstract*— In this paper, a low quiescent current structure with self-regulation impedance buffer and bandgap amplifier is presented. With the bandgap amplifier, the function of voltage reference and error amplifier can be achieved simultaneously, which can efficiently reduce the consumption. The low-dropout regulator has been implemented in a 0.18μm process with die size 0.03mm^2. The circuit module designed in this paper are simulated by the Cadence software and the simulation results are validated. Experimental result shows that the overshoot and undershoot of line transient response are less than 30mV/V. The load regulation is about 0.1%/A, and line regulation is about 0.07mV/V at no load condition. Through the test results, it is found that the simulation results are consistent with the measured data. This conclusion ensures the stability and reliability of this module in the subsequent application scenarios.**

***Index Terms*—low-dropout regulator, adaptive, buffer, bandgap, load capacitor**

I. Introduction

With the more and more demands of the green power IC (integrated circuit), the LDO (low-dropout regulator) with its low power consumption and stable output voltage gets a lot of applications [1-3]. The low quiescent current will restrain the transient response of LDO, and then slow down the transient response speed [6]. This defect will lead to a substantial overshoot or undershoot, even makes the device misoperation or the load damaged. Recent studies proved the Zero-tracking is an effective compensation scheme [7-9], but a larger die size and more power consumption is not up to design requirements. PCA (programmable capacitor array) is also suffered from more die size and high cost [10]. Reference [11] employed the structure with super-source-follower that can decrease the buffer output impedance greatly without much tail current, but the negative feedback loop cannot be stable in all cases, especially when driving a capacitive load. The FVF (flipped voltage follower) is a good method to enhance the transient response but more transistors and current will be consumed [12].

In order to reduce the chip die size, decrease the power consumption and the enhance transient response, a bandgap amplifier with current buffer compensation and self-regulation buffer is proposed to realize a compact LDO [13]. The current buffer compensation can reduce 60% size of the on-chip frequency compensation capacitor without influencing the stability [14]. The output stage of the LDO uses auto adjusting buffer, which can improve the response speed [15]. This design mode can not only simplify the circuit size, but also improve the overall operation efficiency of the application system.

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II. The Proposed LDO structure

To control the quiescent current and reduce the compensation capacitor, the proposed LDO with the bandgap error amplifier (BGEA) and the current buffer scheme is presented. At the same time, the output stage of the proposed LDO using the self-regulation buffer, so it is called BGEA LDO. This scheme can resolve the trade-off among the quiescent current, the chip die size and the transient response.

The traditional LDO usually uses the separate voltage reference and EA. In this paper, the proposed LDO with bandgap amplifier structure is shown in Fig.1. This part contains four circuit modules, which are the startup circuit, the BGEA, the self-regulation impedance buffer and the power MOS MP.

A. Bandgap Error Amplifier Structure

In Fig. 1, the output module is the power stage. In this block, the threshold of the power PMOS MP is higher than that of the NMOS NM_{13}, so the MP can be turned off completely.

The I_{NM13} is the bias current of the output stage in the self-regulation buffer circuit. I_{tail} indicates the charging or discharging current during the transient response. I_D is the dynamic bias current of the self-regulation buffer. I_S is the static bias current of the output stage. As $(W/L)_{NM5}$:$(W/L)_{NM6}$=1:1, when V_{OUT} is regulated at a constant voltage, I_{tail} is zero.

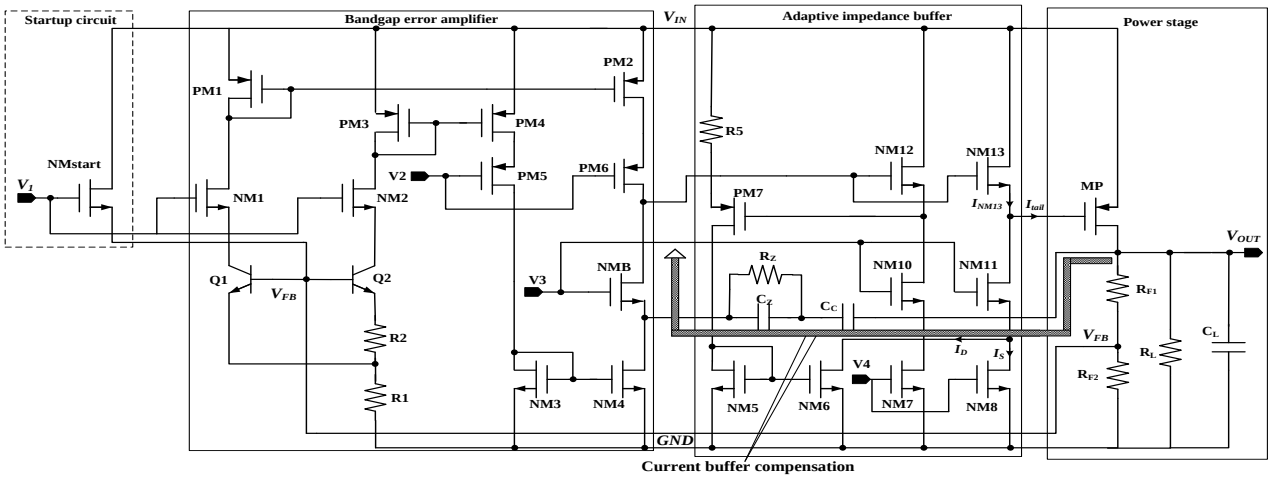


Fig. 1. Schematic of the proposed LDO

$$I_{tail} = I_{NM13} - (I_D + I_S) = 0 \tag{1}$$

In order to analyze the influence of the base voltage on the emission stage current, the simulation result of the relationship between V_{FB} and the current in Q_1 and Q_2 are shown in Fig. 2.

Fig. 2 shows the relationship of the collector current of Q_1 and Q_2 with different V_{FB}. I_{CQ1} and I_{CQ2} are the current flow through the Q_1 and Q_2. g_{mQ1} and g_{mQ2} are trans-conductance of Q_1 and Q_2. The ratio of collector current I_{CQ1} and I_{CQ2} is m: 1. So the current can be shown:

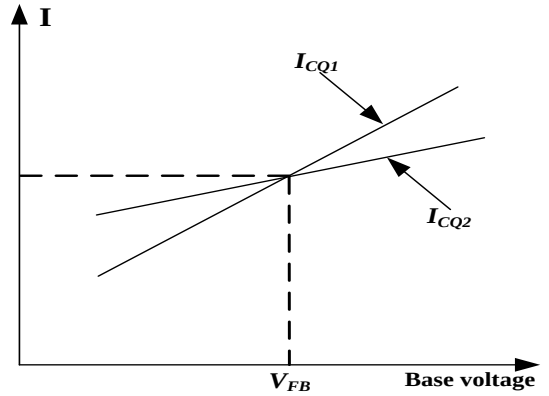


Fig. 2. The relationship of Q_1 and Q_2 with different V_{FB}.

$$I_{CQ_1} = \frac{m \cdot g_{mQ_1}}{m + g_{mQ_1}(m + R_1)} \cdot V_{FB} \tag{2}$$

$$I_{CQ_2} = \frac{g_{mQ_2}}{1 + [g_{mQ_2}(m+1)R_1 + R_2]} \cdot V_{FB} \tag{3}$$

Here, G_{m1} and G_{m2} are the equivalent trans-conductance of Q_1 and Q_2, respectively. The calculation formula is as follows:

$$G_{m1} = \frac{m}{(mR_1 + R_1)} \tag{4}$$

$$G_{m2} = \frac{1}{(1+m)R_1 + R_2} \tag{5}$$

Set $m \geq 1$, it is easy to obtain $G_{m1} > G_{m2}$ and $I_{CQ1} \geq I_{CQ2}$. When V_{FB} gets higher, both currents get bigger, with the faster variation rate of I_{CQ1}. Hence the current variation flow through PM_2 is larger than the current flow through NM_4, then the output of BGEA gets higher. So the feedback loop of the circuit is negative. The base voltage can be fixed at V_{FB} and the V_{OUT} regulation is accomplished. Set $(W/L)_{PM1}:(W/L)_{PM2}=1:1$ and $(W/L)_{NM3}:(W/L)_{NM4}= 1:1$, the trans-conductance g_{mEA} and the output impedance r_{ON1} are:

$$g_{mEA} = G_{m1} - G_{m2} \tag{6}$$

$$r_{ON1} = \left(g_{mNMB} r_{ONMB} r_{ONM4}\right) // \left(g_{mPM6} r_{OPM6} r_{OPM2}\right) \tag{7}$$

The gain of BGEA can be expressed as:

$$gain = g_{mEA} r_{ON1} \tag{8}$$

For the requirement of low quiescent current, the output impedance r_{ON1} of BGEA is about several hundreds of Mega Ohms. Then the gain BGEA is large enough to guarantee the accuracy of output voltage.

B. Adaptive Impedance Buffer

In some proposed works, source-follower buffer is used to separate large output impedance of EA from large parasitic capacitor of the power MOS. The relationship between the output voltage and the buffer load is shown in Fig. 3.

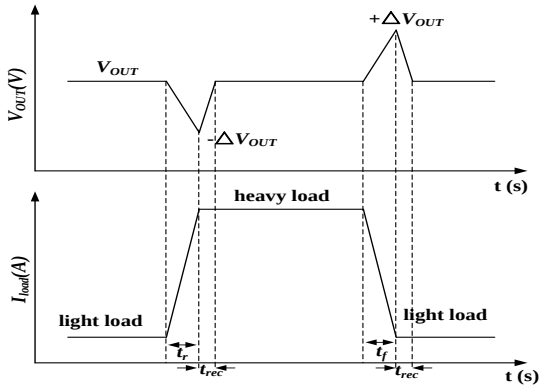


Fig. 3. The variation of V_{OUT} with load

The above graph in Fig. 3 represents the relationship between the V_{OUT} and load, and the below graph is the relationship between the I_{LOAD} and load. When the load is light, the I_{LOAD} is low and the V_{OUT} is high. As the load increases, the I_{LOAD} reaches its maximum when the circuit reaches heavy load. During this process, the V_{OUT} slightly decreases and quickly returns to the original voltage value as the recovery time shortens. Similarly, when the load decreases, the I_{LOAD} changes from a heavy load current to a light load current. At the same time, the V_{OUT} also undergoes a small jump with the load fluctuations and maintaining the original output level within the recovery time immediately. From Fig. 3, the output of the module can still maintain a stable voltage even under high load fluctuations.

Here, the g_{mB} and r_{ON2} are the trans-conductance and output impedance of self-regulation impedance buffer circuit.

$$g_{mB} = g_{mNM13} + \frac{g_{mPM7}}{1 + g_{mPM7} R_5} \tag{9}$$

$$r_{ON2} = \frac{1}{g_{mNM13}} \tag{10}$$

$$\text{Where, } g_{mNM13} = \sqrt{2\mu_n C_{ox} (\frac{W}{L})_{NM13} (I_D + I_S)} \tag{11}$$

The variation of V_{OUT} is $\triangle V_{OUT}$ during the load transient response in Fig.3, $\triangle I_{tail}$ is the charging or discharging current of the power PMOS MP, C_L is the output capacitance of V_{OUT}. t_{rec} is the recovery time, t_r and t_f are the rising time and falling time of I_{load}, respectively.

III. Simulation and Experimental Results

A. Simulation result

The proposed LDO has been implemented in a 0.18 μm CMOS process. In order to coincide with the measured conditions, the capacitance is 0.47 μF and the resistance is 0 Ω here. Fig.4 and Fig.5 show the simulation results of the loop gain transfer function of the proposed LDO for no load and full load, respectively.

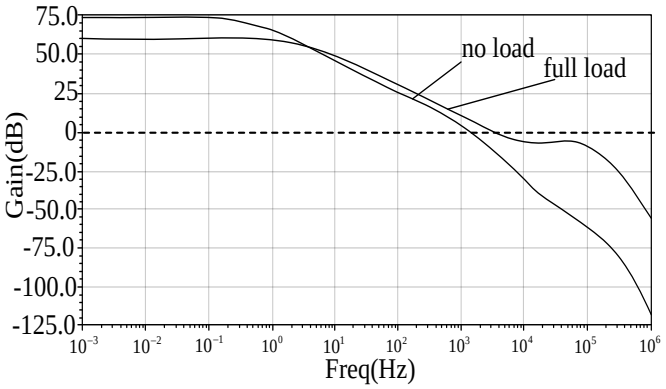


Fig. 4. Gain simulation without load and full load

From the Fig. 4, the load current with the no load and full load conditions, the open loop gain reached 74 dB and 58 dB, respectively.

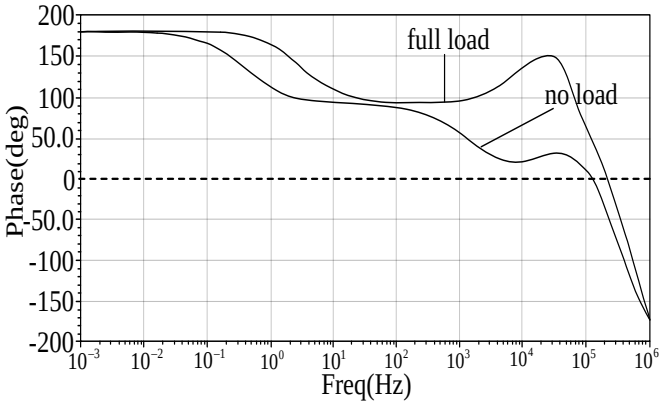


Fig. 5. Phase simulation without load and full load

In the Fig. 5, the load current in the no load and full load, the phase margin is 52 deg and 105 deg, respectively.

In order to represent the phase margin more completely, the simulation results of the circuit at different load currents are shown in Fig. 6.

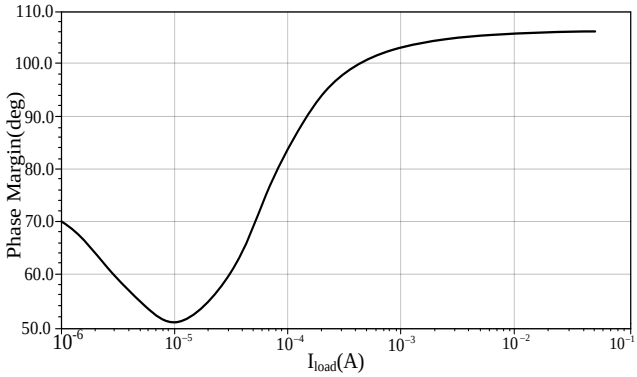


Fig. 6. Phase Margin under different load current

From 1μA~50mA, the simulation results show that the phase margin is always greater than 51deg. It could verify the stability of the system at full load current. Therefore, the LDO is stable with the proposed compensation scheme.

B. Test result

A low ESR 0.47 μF ceramic output capacitor is used to test the performance of the proposed frequency compensation scheme. The chip micrograph is shown in Fig.7.

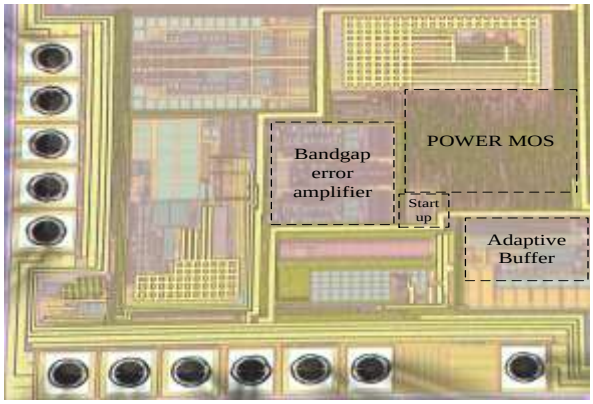
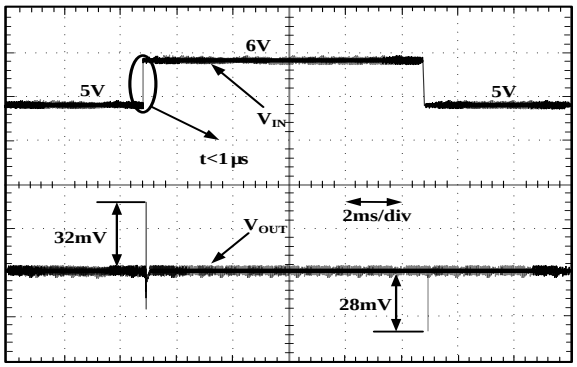
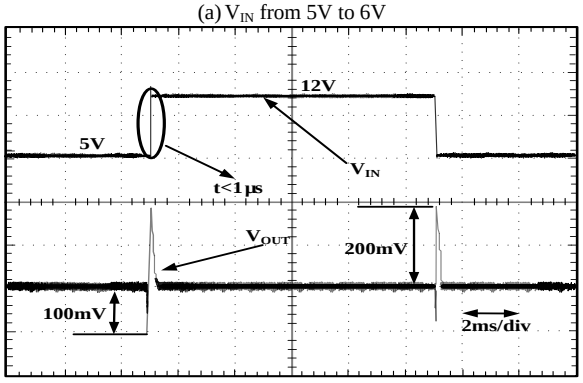


Fig. 7. The chip layout micrograph

To verify transient response of the circuit structure, the linear and the load transient response are measured. The measurement results are shown in Fig. 8 and Fig.9.



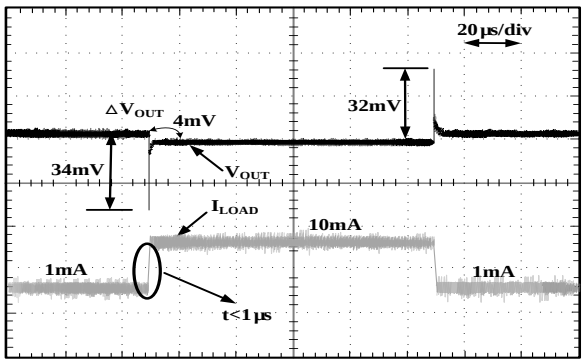
(a) V_{IN} from 5V to 6V



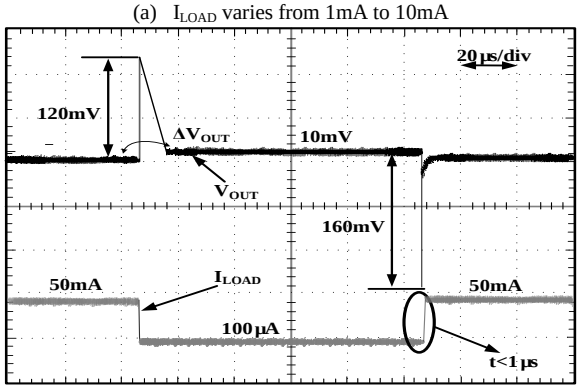
(b) V_{IN} from 5V to 12V

Fig.8 Test result of the linear response (V_{OUT}=1.8V)

In order to better demonstrate the stability of this circuit model, the test will be conducted on the transient responses of voltage and current. From Fig. 8(a), when the input voltage



(a) I_{LOAD} varies from 1mA to 10mA



(b) I_{LOAD} varies from 0.1mA to 50mA

Fig.9 Test result of the load response (V_{OUT}=1.8V)

V_{IN} jumps from 5V to 1V, the maximum fluctuation of the V_{OUT} is 32Mv. With the increasing variation of the V_{IN}, when the V_{IN} jumps from 5V to 12V, the maximum variation of the V_{OUT} is 200mV. The change below the expected indicator is not enough to cause mis-operation in the subsequent circuit.

To test the influence of the I_{LOAD} on $\triangle V_{OUT}$ changes furtherly, it can be seen from in Fig. 9(a), when the I_{LOAD} jumps from 1mA to 10mA, the $\triangle V_{OUT}$ is 34mV. Currently, the I_{LOAD} remains 10mA to 1mA with 100μs, and the $\triangle V_{OUT}$ jumps to 32mV. When the I_{LOAD} jumps greater, the results are shown in Fig. 9(b). When the I_{LOAD} decays from 50mA to 100μA instantly, the $\triangle V_{OUT}$ jumps to 120mV. The I_{LOAD} remains unchanged and jumps from 100uA to 50mA after 100μs, the maximum of the $\triangle V_{OUT}$ is 160mV. It can be seen when the I_{LOAD} changed within 10 times, the output change does not exceed 34mV. When the change in I_{LOAD} reaches 500 times, the maximum output change less than 160mV. The circuit load regulation is about 0.1%/A and it can provide a stable voltage for the back-end circuit. A comparison of some other proposed LDO is given in Table 1.

TABLE I
COMPARISON WITH PREVIOUS REPORTED LDOS

Refs	[6]	[12]	[13]	This work
Technology(μm)	0.35	0.13	0.13	**0.18**
Supply Voltage(V)	3.3	1.2	1.2	**5**
Output Voltage(V)	2.9	1	1	**1.8**
Load Current: I_{Lmax}(mA)	100	50	100	**50**
Quiescent Current: I_q(μA)	55	42	0.7	**9.5**
Load Transient (I_{load} Rising) (mV)	90	140	76	**32**
Load Transient (I_{load} Falling) (mV)	160	80	198	**34**
Load Regulation (mV)	-	10	10	**4**
Line Regulation (mV)	-	30	16.6	**1**
C_L(pF)	100	400	10^6	**$0.47*10^6$**
Year	2016	2019	2020	**2023**

From the Table 1, the LDO presented in this paper realize the minimum quiescent current, chip die size and small off-chip capacitor.

IV. CONCLUSIONS

This paper proposes a compact and ultra-low power LDO architecture. Based on the main principle of the bandgap comparator and error amplifier of the traditional LDO, a bandgap error amplifier with high temperature compensation is proposed. Then the adaptive impedance follower is analyzed. It can adjust the output resistance with the different output load currents, which increases the transient response speed of the circuit while ensuring stability. The LDO circuit structure proposed in this paper can not only reduce the quiescent current efficiently, but also compensate the temperature of the output voltage. Based on the adaptive impedance follower architecture, the compensation scheme is used to obtain the stability of the loop within the full load current variation range, which can achieve low quiescent current and increase the transient response speed at the same time.

In this contribution, the fabricated structure of the LDO with the adaptive impedance buffer could improve the transient response remarkable. Compared with the traditional LDO, the proposed LDO consume 1μA quiescent current in

the no load condition and 10 μA quiescent current even in the full load. Meanwhile the LDO can realize good stability under full range of load current using the current buffer compensation. The circuit can realize as large as 50mA load current with input voltage range between 2.5V and 30V. So, the LDO circuit has good linear response characteristics. When the output swing between 4~10mV, the load regulation meets the design requirements. By comparing the parameters with the similar circuits, the LDO designed in this paper has lower quiescent current and smaller layout area. It can be used in a variety of consumer electronic products.

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