

A Topology of Current-limiting Hybrid DC Circuit Breaker Based on Auxiliary Capacitor Commutation

Baoge Zhang, Yuan Wang, Shaoning Li and Li Ma

Abstract—To address the issues of the suppressing and the eliminating fault currents in direct current transmission networks, and to reduce the persistently high costs of high-voltage direct current circuit breakers, a low-cost and effective current limitation hybrid direct current circuit breaker topology based on auxiliary capacitors is proposed. Which can implement current limiting and rapid disconnection during the occurrence of faults in the DC power grid. In the topological design, thyristors and auxiliary capacitors work in coordination to provide a tripping command for the ultra-fast mechanical switch (UFMS) and quickly engage the current-limiting branch composed of a capacitor branch to suppress the fault current. This topology adds a capacitor branch and reduces the number of IGBT branches, offering certain economic benefits. At the same time, it introduces a bypass branch that reduces the energy consumption as much as possible for the surge arrester and increases the switching speed of the circuit breaker. The content of the current-limiting has been analyzed through circuit state derivation and the proposed circuit breaker has been conducted, including the fault clearing time, the maximum peak value reached during a fault, the stress on the energy dissipation of the surge arrester, building a 500kV Four-Terminal DC System Simulation Circuit Based on PSCAD/EMTDC. A comparative analysis with existing typical schemes is also conducted, and the results demonstrate the topology has smaller current values, shortened breaking times, and significant cost reduction.

Index Terms—Direct current transmission, Hybrid DC circuit breaker, Auxiliary capacitor, Current-limiting branch, Bypass branch

I. INTRODUCTION

IN recent years, due to the rapid progress of power electronics technology, and extensive popularization of new energy sources, Modular Multilevel Converter (MMC) technology for flexible DC grids is in the limelight [1]. The proportion of new energy power applications has increased, the application of high-voltage direct current transmission system is also expanding year after year to improve the

efficiency of power transmission. High-voltage direct-current transmission usually uses overhead lines [2]. Exposure of overhead lines to the natural environment increases the risk of line failures [3],[4]. DC grids are characterized by lower inertia and lower impedance[5], Which leads to a rapid increase in current when a fault occurs, posing a serious event for the stable work of the power grid. So quickly and safely cut off the fault which becomes one technology to ensure the stable operation of direct current system [6], [7].

Currently, high-voltage direct current circuit breakers has been categorized into three types: mechanical direct current circuit breaker [8],[9], solid-state direct current circuit breaker [10],[11] and hybrid direct current circuit breaker [12],[13]. Compared to the mechanical direct current circuit breaker and solid-state direct current circuit breaker, hybrid direct current circuit breaker combine the advantages of both mechanical types and solid-state types, with low on-state losses, rapid breaking capacity and excellent reliability. Hybrid direct current circuit breakers have become the preferred solution in numerous significant projects both domestically and internationally. In 2012, ABB company developed and manufactured the first 320kV hybrid direct current circuit breaker with 9kA/5ms of world [14]. In 2014, the Global Energy Internet Institute developed a hybrid direct current circuit breaker that utilizes rapid mechanical switching and cascaded full-bridge modular technology. It was successfully practiced to the Zhoushan flexible current circuit grid transmission scheme in 2016 [15]. In 2019, the Zhangbei flexible direct current grid adopted a 535kV direct current circuit breaker which has the highest voltage level in the world [16]. Nanrui Jibao, Global Energy Internet Research Institute, China Xidian Group and other units have successfully developed 500kV high-voltage current circuit breakers and carried out research on the corresponding test technology [17], which is planned to be used to the Zhangbei four-terminal flexible DC transmission scheme [18]. Hybrid high-voltage direct current circuit breakers play a key role in the applied research field with high-voltage, large-capacity and long-distance flexible DC grids.

As the voltage level of the DC transmission system increases, it becomes especially critical to reduce the fault currents when a fault could occur. Superconducting techniques were used to limit the current, However, the immaturity and high cost of superconducting technology make it difficult to be widely used in practical engineering [19]. The H-bridge type structure is used which allows the circuit breaker to turn on and off the current in both directions, thus reducing the need for IGBT devices by half [20].

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Nonetheless, a large number of series-connected IGBT devices are still required, and the cost is still high. In addition, a current-limiting topology about hybrid direct current circuit breaker is proposed, but which relies on a direct current reactor in the line to limit the value of the current [21].

Combined with the fact that our power grids are a large regional grids constructed by transmission lines with 500 kV. In order to better suppress short-circuit currents and reduce the high cost of high-voltage direct current circuit breaker, A new capacitor-commutated current-limiting hybrid direct current circuit breaker topology applied to 500 kV transmission lines is proposed by the paper. The proposed topology has capacitors, which can replace the original IGBTs transfer circuit, thus effectively reducing the used IGBTs numbers, greatly reducing the circuit breaker manufacturing cost. Short-circuit currents are effectively suppressed by combining the current-limiting branches of capacitors, inductors and resistors. In addition, the bypass branch effectively reduces the arrester's absorbed energy and lowers the design specification of the arrester. Then, the simulated model are done in PSCAD platform for simulation and comparison, which verifies the new feasible topology has better cost.

II. TOPOLOGY AND WORKING PRINCIPLE

2.1 Topology

The proposed topology with capacitor commutated and current limiting function (CLCC-DCCB) is shown in Fig. 1. which is divided into some parts through current branches, limited current branch, current breaking branches and bypass branch, and Bidirectional fault shutdown is implemented by the full-bridge structure.

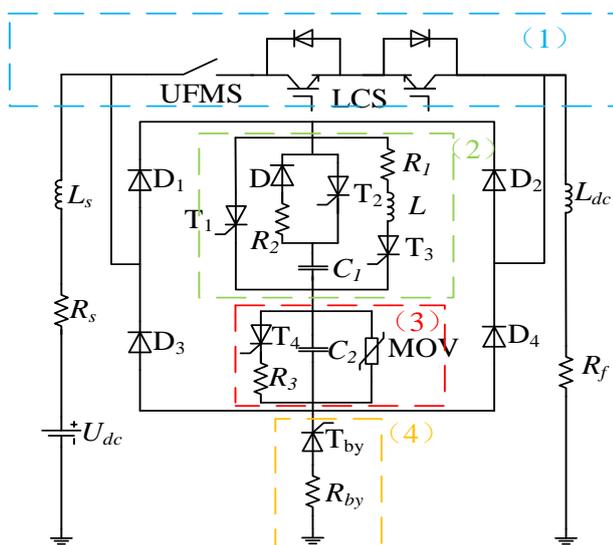


Fig. 1 Topology of CLCC-DCCB.

(1) The through-current branches consist of one ultrafast disconnector (UFMS) , one load commutation switch (LCS), where the LCS consists of an IGBT reverse parallel diode to carry the current when it is in normal work.

(2) The current-limiting branches consist of three sets of thyristors, one set of current-continuing diodes, a current-limiting resistor, an energy-discharging resistor, a current-limiting inductor, and a pre-charging capacitor. The pre-charge capacitor ensures reliable shutdown of T₁ and also

prevents over-voltage on both sides of the current-limiting inductor, allowing the current-limiting inductor to be smoothly introduced into the circuit.

(3) The current-break branches circuit consist of an energy-drain resistor R₃, a set of thyristors, a surge arrester and a capacitor. When the voltage across the capacitors reache the arrester working voltage, which acts to absorb the fault energies and break this fault current.

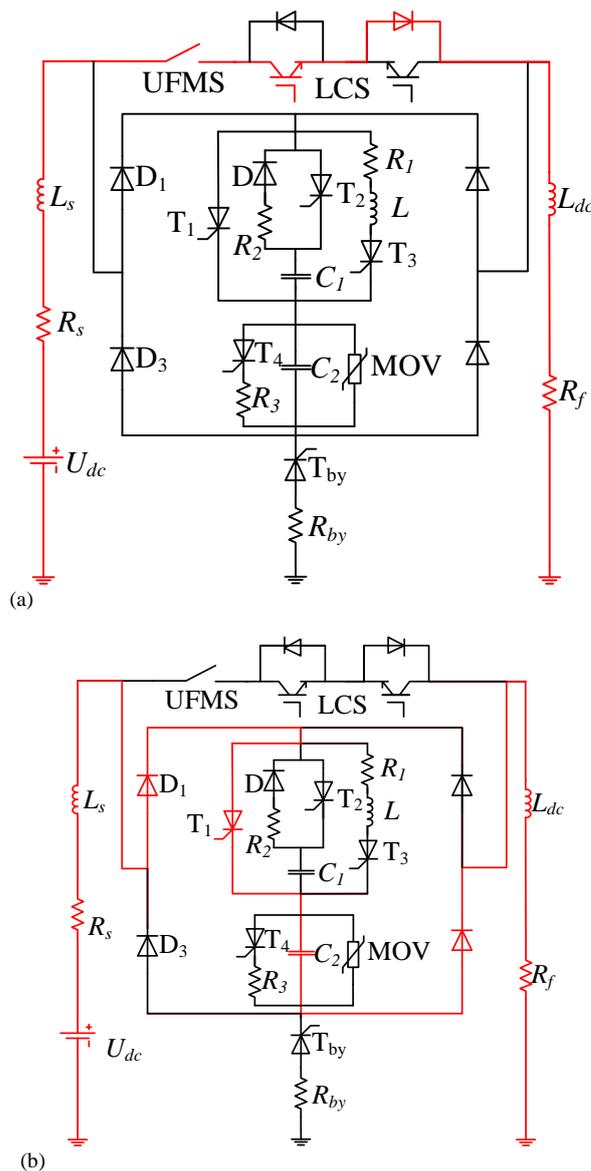
(4) The bypass branch consists of a set of thyristors T_{by} and energy-dissipating resistors R_{by}. When the lightning arrester operates, the thyristor conducts, then the dissipative resistor absorbs the energies of the fault-side inductance, which reduces the lightning arrester can absorbe energies.

2.2 Working Principle

The CLCC-DCCB fault current transfer paths are shown in Fig. 2.

2.3 Low-current interruption mode

When the power system experiences a small current fault caused by a high resistance ground fault, the fault current is not significant and minimal impact on the system. Therefore, there is no need to limit the current value current, so which could be interrupted directly. In this mode, the action process from t₀ to t₂ is the same as that in the current-limiting interruption mode.



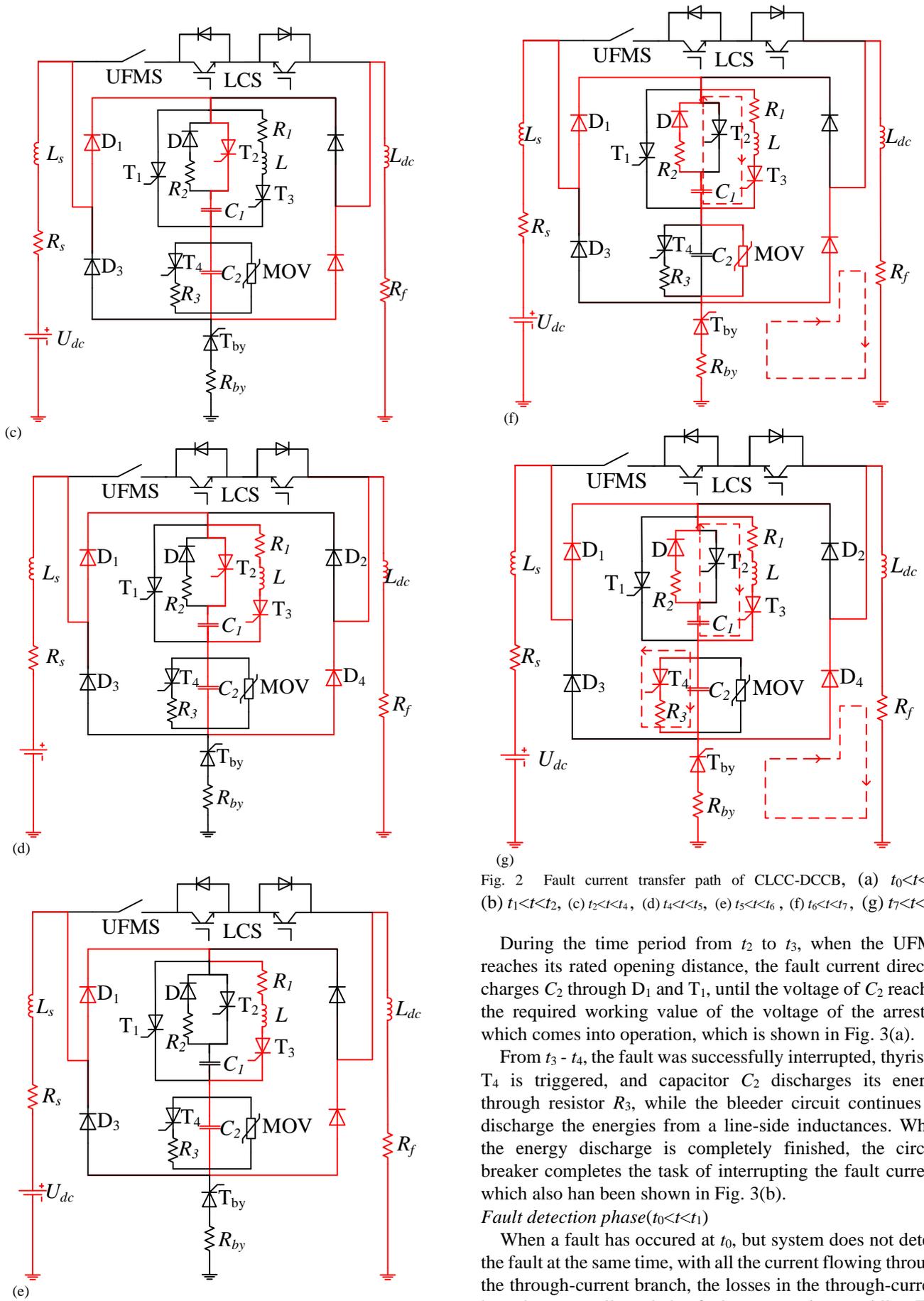


Fig. 2 Fault current transfer path of CLCC-DCCB, (a) $t_0 < t < t_1$, (b) $t_1 < t < t_2$, (c) $t_2 < t < t_4$, (d) $t_4 < t < t_5$, (e) $t_5 < t < t_6$, (f) $t_6 < t < t_7$, (g) $t_7 < t < t_8$.

During the time period from t_2 to t_3 , when the UFMS reaches its rated opening distance, the fault current directly charges C_2 through D_1 and T_1 , until the voltage of C_2 reaches the required working value of the voltage of the arrester, which comes into operation, which is shown in Fig. 3(a).

From $t_3 - t_4$, the fault was successfully interrupted, thyristor T_4 is triggered, and capacitor C_2 discharges its energy through resistor R_3 , while the bleeder circuit continues to discharge the energies from a line-side inductances. When the energy discharge is completely finished, the circuit breaker completes the task of interrupting the fault current, which also has been shown in Fig. 3(b).

Fault detection phase ($t_0 < t < t_1$)

When a fault has occurred at t_0 , but system does not detect the fault at the same time, with all the current flowing through the through-current branch, the losses in the through-current branch are small, and the fault current rises rapidly. The current during normal operation of the system is Recorded as I_0 , the fault current during the period t_0-t_1 is

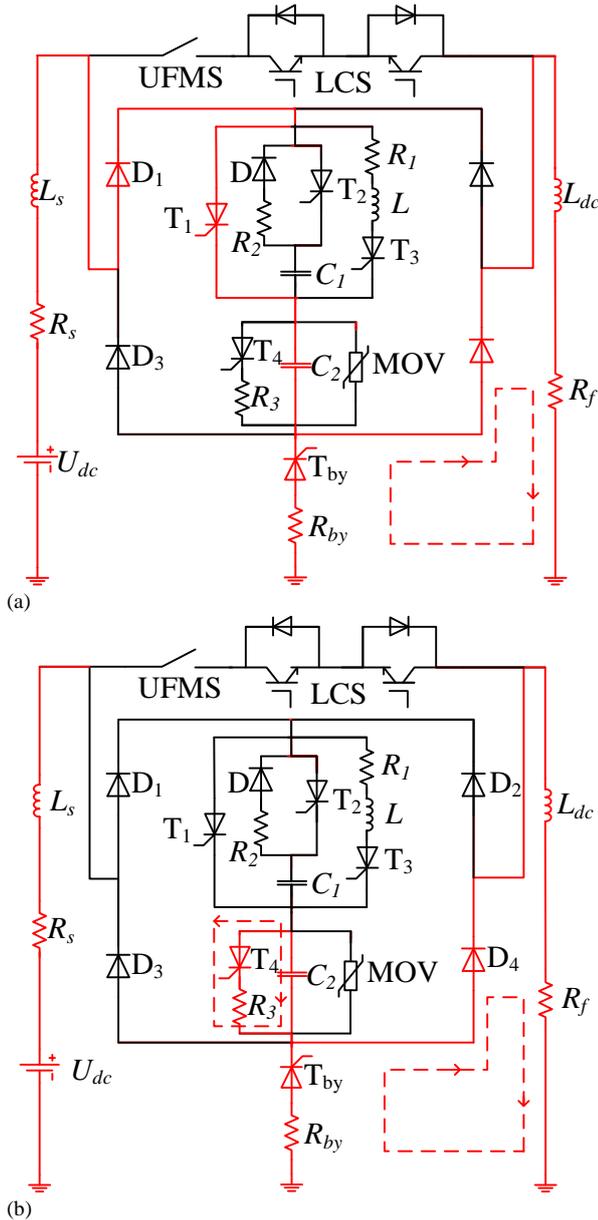


Fig. 3 Process of breaking a small current, (a) $t_2 < t < t_3$, (b) $t_3 < t < t_4$.

$$i_{dc} = I_0 e^{-(t-t_0)/\tau_1} + \frac{U_{dc}}{R_s + R_{line}} (1 - e^{-(t-t_0)/\tau_1}) \quad (1)$$

In the formula, the time constant refers to

$$\tau_1 = (L_s + L_{dc}) / (R_s + R_{line})$$

Fault current transfer phase ($t_1 < t < t_2$)

The system detects a fault at the moment t_1 . Conducting the thyristor group T_1 of the system branch and the converter capacitor C_2 of the system, while giving the fast mechanical switch UFMS the command to open the gate. Gives a load transfer switch (LCS) shutdown command, so that the current of the system fault can be transferred from the through-current branch, which can go to the circuit breaker. Neglecting the voltage drop of the power electronics and considering it as an ideal component. According to Kirchhoff's voltage law (KVL), equation is obtained, as in

$$\begin{cases} U_{dc} = L_0 \frac{di_{dc}}{dt} + R_0 i_{dc} + u_{C_2} \\ i_{C_2} = i_{dc} = C_2 \frac{du_{C_2}}{dt} \end{cases} \quad (2)$$

Where, $L_0 = L_s + L_{dc}$, $R_0 = R_s + R_{line}$, From equation (1), it can be derived that $i_1(t_1) = i_{dc}(t_1) = I_1$, which is taken into equation (2), then

$$i_{C_2} = i_{dc} = e^{-\alpha(t-t_2)} (U_{dc} C_1 \omega \sin(\omega(t-t_2)) - I_2 \sin(\omega(t-t_2) - \beta)] \quad (3)$$

$$\text{Where, } A = \frac{R}{2L_0}, \omega_0 = \sqrt{\frac{1}{L_0 C_2}}, \alpha = \arctan \frac{\omega}{A},$$

$$\beta = \arctan(\omega / \alpha)$$

Preparation phase for current limitation ($t_2 < t < t_4$)

When it is confirmed that the fast mechanical switch UFMS breaks the gate to reach the rated opening distance, giving the thyristor group T_2 trigger signal, then T_2 is subjected to a forward voltage, then the capacitor C_1 in the current-limiting circuit conduct. Because the initial voltage of C_1 is inverse to the voltage of the line, the capacitor begins to discharge firstly, because of the backpressure, the anode current flowing through T_1 drops rapidly, the fault current can be gradually transferred from the T_1 branch to T_2 , until which flowing through T_1 becomes 0A at the moment t_3 , T_1 is successfully turned off by T_2 . However, when the current of T_1 becomes 0A, T_1 still needs to bear the reverse voltage, which will keep a certain time for it to recover its blocking ability to the forward voltage, and tens of microseconds is needed for a fast thyristor turn-off, the capacitor discharge ends at the moment T_4 . Let the value of the precharge voltage of C_1 be U_0 , because the turn-off of T_1 is very rapid, so the turn-off time is negligible, it can be considered that at the moment of t_2 the current then can be all transferred to the T_2 branch, through Kirchhoff's voltage law (KVL), equation is obtained, as in

$$\begin{cases} U_{dc} = i_2 R + L \frac{di_2}{dt} + U_{c2} - U_{c1} \\ i_2 = i_{c1} = i_{c2} = -C_1 \frac{du_{c1}}{dt} \end{cases} \quad (4)$$

At this time, from equation (3), the current value at the moment t_2 is calculated as $i_2(t_2) = I_2$, it is brought into equation (4), then

$$U_{C_1} = (U_{dc} + U_0) \cos(\gamma(t-t_3)) - \frac{I_2}{C_1 \gamma} \sin(\gamma(t-t_3)) - U_{dc} \quad (5)$$

$$i_{C_1} = (U_{dc} + U_0) C_1 \gamma \sin(\gamma(t-t_3)) + I_2 \cos(\gamma(t-t_3)) \quad (6)$$

$$\text{Where, } \gamma = \sqrt{\frac{C_2 + C_1}{C_1 C_2 L_0}}$$

Current limiting start phase ($t_4 < t < t_5$)

At the moment t_4 , the discharge phase of capacitor C_1 has been all completed, at the same time, then the voltage across the C_1 capacitor is 0V, that is $U_{C1}(t_4) = 0V$. After the moment t_4 , capacitor C_1 starts charging in the reverse direction, at this time, T_3 conducts because of the positive voltage, and the resistive branch begins to put into operation, according to Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL), equation can be obtained

$$\begin{cases} U_{dc} = L_0 \frac{di_{C2}}{dt} + R_0 i_{C2} + u_{C1} + u_{C2} \\ u_{C1} = -L \frac{di_L}{dt} - R_L i_L \\ i_{C1} = -C_1 \frac{du_{C1}}{dt} \\ i_{C2} = i_{dc} = i_{C1} + i_L \end{cases} \quad (7)$$

The simplification is obtained

$$\frac{C_1 C_2}{C_1 + C_2} L_0 \frac{d^2 u_C}{dt^2} + \left(\frac{L_0 + L}{L} \right) u_C + U_{dc} = 0 \quad (8)$$

From equation (6), the current initial value at the moment t_4 is $i_{C1}(t_4)=i_{dc}(t_4)=I_3$, substituting the initial value $U_{C1}(t_4)=0V$, $i_{C1}(t_4)=I_3$, into equation (7), then

$$\begin{cases} i_{C1} = AC_1 \lambda \sin[\lambda(t-t_4)] + I_3 \cos[\lambda(t-t_4)] \\ u_{C1} = \frac{-I_3}{\lambda C_1} \sin[\lambda(t-t_4)] + A[\cos \lambda(t-t_4) - 1] \\ i_L = -\frac{A}{\lambda} [\sin(\lambda(t-t_4)) - \lambda(t-t_4)] \\ \quad + B[1 - \cos(\lambda(t-t_4))] \end{cases} \quad (9)$$

Where, $A = \sqrt{LU_{dc} / (L + L_0)}$, $B = I_3 / LC \lambda^2$, $C = C_1 C_2 / (C_1 + C_2)$.

The capacitor C_1 voltage increases as the duration of charging increases, and the current flowing through capacitor C_1 becomes smaller and smaller. The capacitor C_1 voltage reaches the rated the system voltage, then the capacitor C_1 is disconnected from the system.

Current limiting fully committed phase ($t_5 < t < t_6$)

The resistive branch is fully operational in the system at the moment t_5 . Equation (9) shows that the fault current through the inductive load branch is equal to the actual fault current through the circuit breaker at this moment of t_5 , that is $i_L=i_{dc}=I_4$, according to KVL and KCL, equation is obtained

$$i_L = I_4 e^{-(t-t_5)/\tau_0} + \frac{U_{dc}}{R_\Sigma} (1 - e^{-(t-t_5)/\tau_0}) \quad (10)$$

Where,

$$\tau_0 = (L_0 + L) / R_L, \quad R_\Sigma = R_L + R_s + R_f.$$

Stream break phase ($t_6 < t < t_7$)

As the voltage of C_2 becomes higher and higher, the voltage of C_2 from the moment t_6 reaches the arrester operation voltage value, then which is put into operation for absorbing the voltage on the non-faulted side. Meanwhile, it the diversion branch thyristor T_{by} is triggered to conduce, and the diversion branch is used to discharge the fault energy of the system by the grounding resistor R_{by} , the diversion branch circuits reduce the amount of energy released by the arrester. Capacitor C_1 forms a discharge loop with the resistive inductive branch and diode D, in this process, capacitor C_1 is discharged and then charged. At the moment of t_7 , the current through the arrester is 0A, the arrester's energy absorption phase is over, and the fault is successfully cut off.

Denoting the time of lightning arrester operation during the time t_6 - t_7 as Δt , from equation (10), the initial value of the current at the moment t_7 is $i_{dc}(t_7) = I_5$, the arrester starting operating voltage is U_{MOV} , according to KVL, then

$$i_{dc} = I_5 e^{-\Delta t/\tau_1} + \frac{U_{dc} - U_{MOV}}{R_s + R_L} (1 - e^{-\Delta t/\tau_1}) \quad (11)$$

$$\Delta t = -\frac{L + L_s}{R_L + R_s} \ln \frac{\Delta U}{(R_L + R_s) I_7 - \Delta U} \quad (12)$$

Where, $\tau_1 = (L + L_s) / (R_L + R_s)$, $\Delta U = U_{dc} - U_{MOV}$.

Drain phase ($t_7 < t < t_8$)

The current through the arrester at the moment t_7 is zero, and the system fault side current value can be continued to release energy by the grounding resistor, due to the shutdown, non-fault side current becomes 0A, at this moment, the thyristor T_4 is energized, so that capacitor C_2 is discharged through the energy-discharging resistor R_3 . Capacitor C_1 continues the charging and discharging process, at the moment t_8 , the operation of all circuits is completed and the circuit breaker ends its operation.

III. DEVICE PARAMETERIZATION

According to the circuit breaker action process, the current limiting inductor natural input can be realized through the auxiliary capacitor C_1 , the operation of the arrester is controlled by capacitor C_2 . In order to avoid excessive withstand voltage requirements, the parameters of the devices in the proposed circuit breaker should be set appropriately. The equivalent voltage of the designed direct current grid of the paper is 500 kV, according to this standard, the parameters of the primary devices of the circuit breaker han been well designed. In this section, by analyzing the parameters of capacitors C_1 and C_2 , L is current-limiting inductor, and R_1 is current-limiting resistor, and R_3 is current discharge resistor, and then the optimal parameters for each component are determined.

3.1 Selection of capacitor parameters

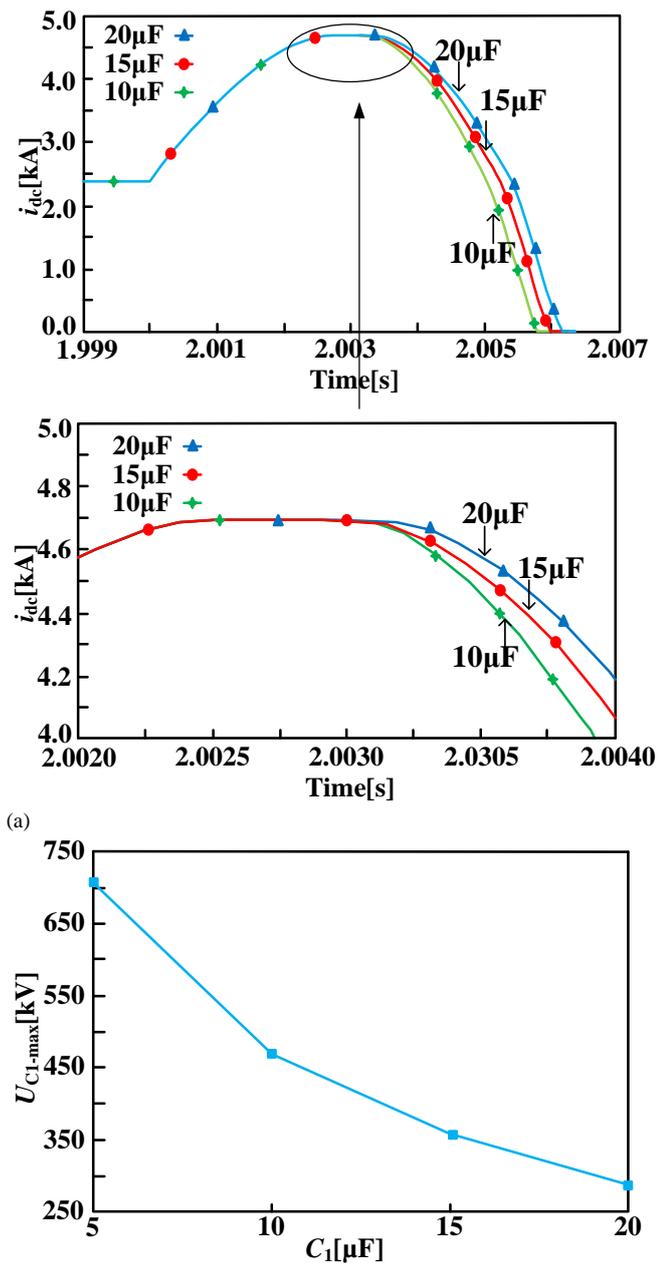
3.1.1 Parameter selection of capacitor C_1

The selection of capacitor C_1 is focused on the speed of the circuit breaker's operation and a good voltage withstand level of the device. The larger the capacitor C_1 values, the more energy is transferred from the DC supply, the longer period the capacitor takes to charge, and the longer period it occupy for the resistor and reactance to be located to be fully engaged, and therefore the longer time the fault current is turned off. In the paper, based on the 500kV DC system, a relationship between the breaking current with this capacitance C_1 parameters is revealed in Fig. 4(a).

Fig. 4(b) shows the relationship between this capacitor C_1 parameters and the forward voltage maximum value of capacitor C_1 . According to Fig. 3(b), which can be found that the smaller these capacitance values, the larger the capacitor C_1 maximum voltage, and therefore the higher the voltage withstand levels of the circuit components is required. The capacitor C_1 cost increases exponentially when the voltage level is higher. Taking the cost and the opening time into consideration, the value of capacitor C_1 is taken to be 15 μF .

3.1.2 Parameter selection of capacitor C_2

The function of capacitor C_2 in the circuit breaker is to control the operation of the arrester, when the voltage across C_2 reaches the operating voltage of the arrester, the arrester conducts, the current is transferred to the arrester, and capacitor C_2 is disconnected.



(b) Fig. 4 Influence of capacitance C_1 value, (a) relationship between C_1 and i_{dc} , (b) relationship between C_1 and U_{C1-max} .

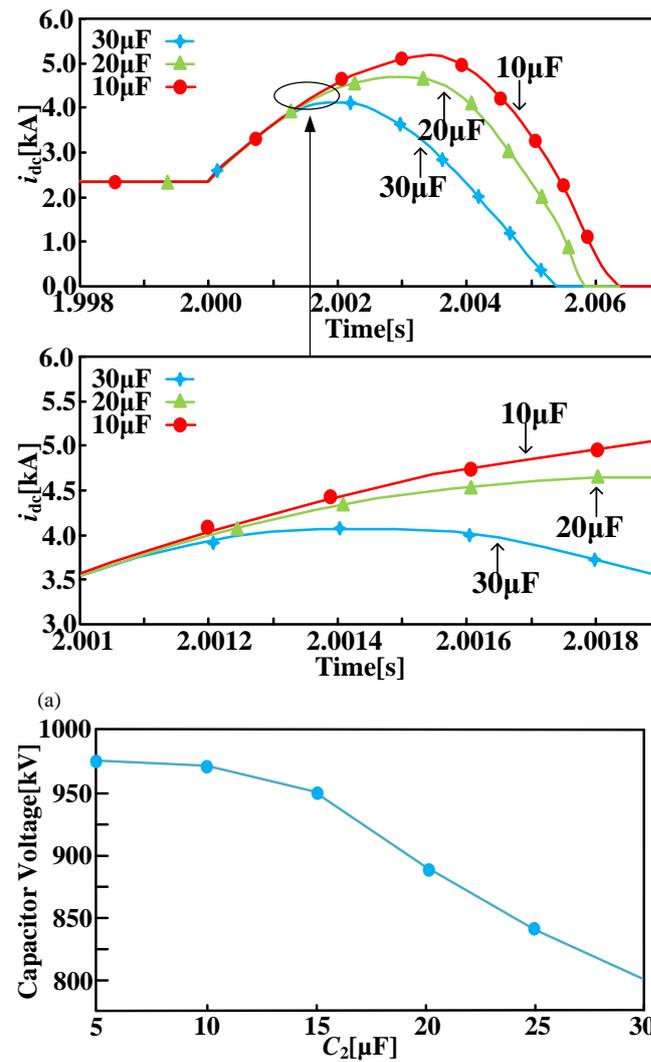
From Fig.5(a), it can be seen that the larger capacitance value of capacitor C_2 , the longer time this circuit breaker breaks the short-circuit current, the higher these short-circuit current peak values. However, the smaller capacitance of capacitor C_2 , the higher circuit voltage and the higher withstand level for power electronic circuits, which leads to increasing the cost. To sum up, the value of capacitor C_2 in the paper is selected as 20 μF .

3.2 Parameter selection of current-limiting inductor

Current-limiting inductors can restrain the fault current rise rate. The larger the current-limiting inductor, the more effective it is in suppressing fault currents, but it also extends the time it takes for the inductor to become fully engaged, lead to the circuit breaker to take longer to break.

Since the size of the applied flat wave reactor L_{dc} in the project is 150 mH. According to the actual rated voltage of the DC grid of 500 kV, so the actual value of the current

limiting inductance is given to be between 150-300 mH. As



(b) Fig. 5 Influence of capacitance C_2 value, (a) relationship between C_2 and i_{dc} , (b) relationship between C_2 and circuit voltage.

shown in Fig. 6, the larger this inductor L values, the longer it will spend time for capacitor C_1 , which carries on to reverse charging to a maximum voltage, which also obviously indicates the larger these inductance values, the longer the inductance will take for the current limiting inductor branch to become fully operational, the larger these voltage values of capacitor C_1 are going to be, and the high voltage reactance cost can be very costly, therefore, in 500kV DC grid, this current limiting resistive inductor of this branch is used about 200 mH inductor.

3.3 Parameter design of current limiting resistor R_1

According to Fig. 7(a), a phenomenon can be found this current limiting resistor resistance is inversely proportional for this voltage of capacitor C_1 , directly proportional to the charging time of capacitor C_1 . However, it objectively show that the effects of R_1 own volume and heat dissipation is taken into account, so the resistance value of R_1 cannot be increased indefinitely. The current limiting resistor can inhibit the rising rate of the short-circuit current, and from Fig. 7(b) it objectively is shown the larger this current limiting resistor is, the larger the peak inhibition of the short-circuit current is, and the larger the peak inhibition of the short-circuit current is. A resistance value of 10 Ω is used as the resistor R_1 .

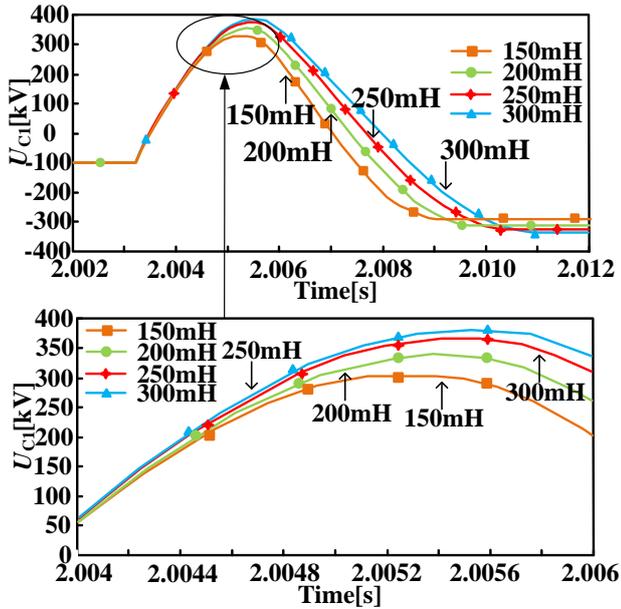


Fig. 6 Influence of current limiting inductors value.

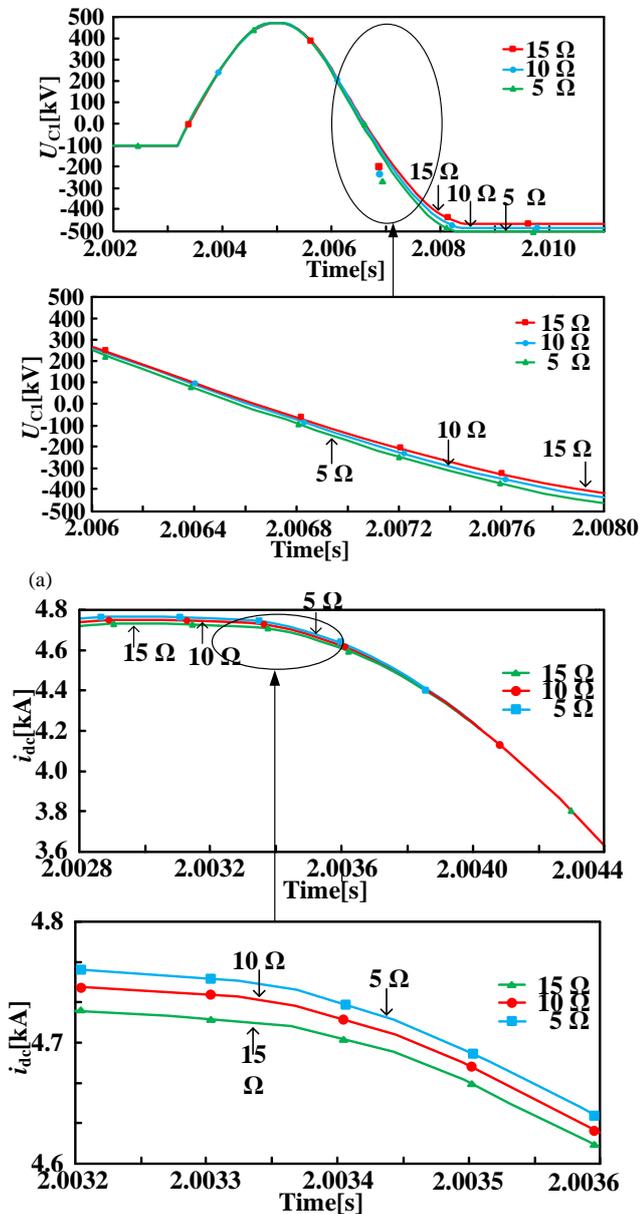


Fig. 7 Influence current limiting resistance R_l value, (a) relationship between R_l and U_{cl} , (b) relationship between R_l and i_{dc} .

3.4 Parameterization of Drain Resistor R_3

When the fault is successfully isolated, thyristor T_4 conducts and capacitor C_2 discharges its own energy through energy-discharging resistor R_3 . When the energy is drained, the current in the energy drain circuit becomes 0A. Thyristor T_4 is disconnected, then this circuit breaker returns to its initial state. According to Fig. 8, it can be seen that when the leakage resistance is larger, the current of the energy discharging branch is smaller, and the energy discharging time of the energy-discharging branch is also longer. Considering the size and heat dissipation of the energy discharge resistor, the resistance value of the energy discharge resistor cannot be increased indefinitely. Focusing on the energy-discharging circuit peak current, the length of the energy discharging time, the resistance value of the energy discharging resistor should not be too large or too small, so in the paper 100Ω is selected as the resistance value of the energy-discharging resistor.

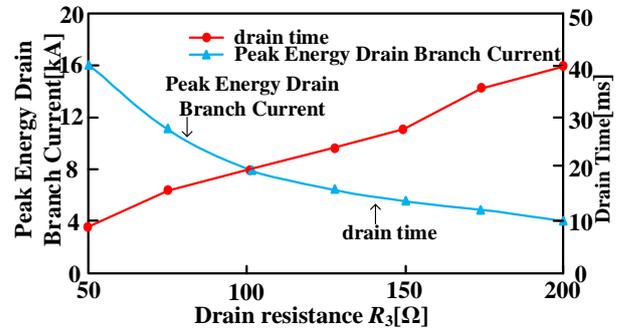


Fig. 8 Influence of energy discharge resistance R_3 value.

3.5 Lightning arrester parameter selection

The arrester is connected in parallel to the converter capacitor C_2 , when the voltage of capacitor C_2 reaches the arrester starting voltage, the surge arrester discharges energy from the short-circuit current.

In the paper, the proposed topology is applied to a 500kV DC transmission system, thus the rated voltage value of a surge arrester is taken between 400kV and 600kV.

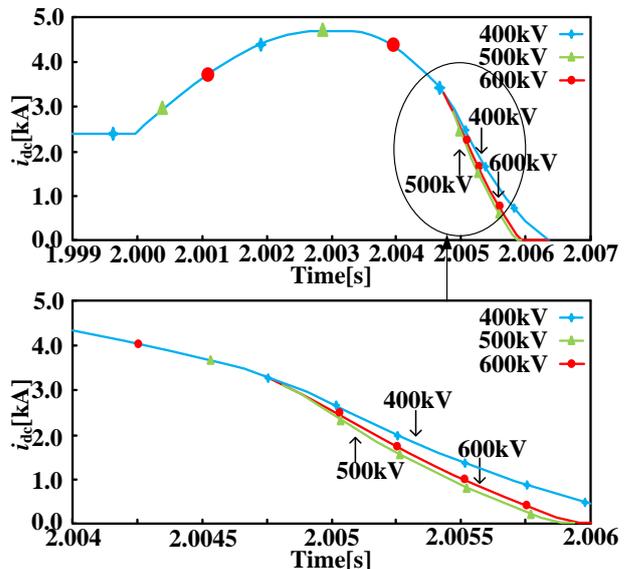


Fig. 9 Effect of Arrester Rated Voltage on Breaking Time.

According to Fig. 9, it can be seen that the greater the rated

voltage of the arrester, the shorter the opening time of this fault current, however, along with the higher the rated voltage of the applied arrester, then going on, the higher these voltage values applied to the ends of the converter capacitor C_2 , lead to the cost of capacitors increases exponentially at high voltages. Considering the opening time and cost, in the paper 500kV is selects as the rated voltage of the arrester.

IV. SIMULATION ANALYSIS

4.1 Simulation analysis

To examine the current limiting and fault current breaking performance of the based on capacitor commutated hybrid DC circuit breaker, the 500kV four-terminal DC system simulation model is constructed through the PASCAD software, and these simulation parameters are shown in Table I, and the simulation diagrams are shown in Fig. 10.

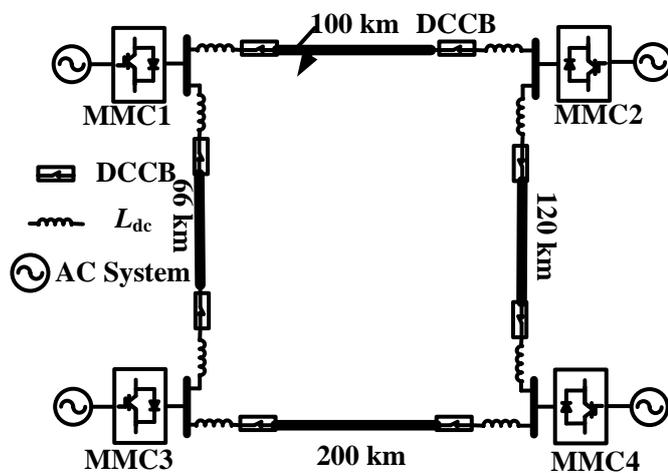


Fig. 10 Simulation model of four terminal bipolar DC power grid.

When selecting individual devices, the device models of ABB company are adopted, so the selected IGBT model is 5SNA3000K452300, it's rated voltage and current are concrete knowable about 4.5 kV/3 kA, and the selected thyristor model is 5STP45Y8500, it's rated voltage and current are concrete knowable about 8.5 kV/4.5 kA, these selected diode model is 5SDD40H4000, it's rated voltage and current are concrete knowable about 4.5 kV/3.8 kA. In the paper, the current limiting capacitor C_1 can be designed to be about 10 μ F, the commutation capacitor C_2 can be devised about 20 μ F, the current limiting resistor R_1 of the breaker is designed to be 10 Ω , the current limiting inductor L of the breaker is designed to be 200 mH, and the energy dissipation resistor R_3 is designed to be 100 Ω .

TABLE I
SIMULATION PARAMETERS OF DC POWER GRID

System parameters	MMC1	MMC2	MMC3	MMC4
Converter capacity/ MW	1500	1000	3000	1500
Submodule capacitance/ μ F	7000	15000	15000	7000
Bridge Arm Inductors /mH	100	50	50	100
Level wave reactance/ mH	200	200	200	200

4.2 Fault Clearance Simulation

The current transfer process of the proposed circuit breaker breaking fault in the paper is shown in Fig. 11.

The Fig. 11 shows that a short-circuit fault turns up at $t=2.0$ s (t_0 moment), at this time the system has not detected the short-circuit fault, When 1ms has passed, the system detects the fault. at $t=2.001$ s (t_1 moment) time the thyristor T_1 conducts, the commutation capacitor C_2 is introduced into the branch circuit, UFMS begins to close, but UFMS takes 2ms to reach rated breaking distance. At $t=2.003$ s (t_2 moment), the current-carrying branch is completely shut down because the UFMS has reached its rated breaking distance. At the same time, the thyristor T_2 is given a trigger signal to turn on, and the capacitor C_1 starts discharging. At $t=2.0034$ s (t_3 moment), T_1 is subjected to reverse voltage shutdown. At $t=2.0035$ s (t_4 moment), the capacitor C_1 discharge is completed, and begins to charge in the reverse direction. The current-limiting branch take positive voltage to conduct. At $t=2.0048$ s (t_5 moment), the current limiting branch is fully operational. At $t=2.0052$ s (t_6 moment), the arrester reaches the turn-on voltage and begins to dissipate energy. At the same time thyristor T_{by} quickly conducts and the bypass branch consumes the fault side energy. At $t=2.0058$ s (t_7 moment), the short-circuit current becomes 0A, then fault is cleared, and the bypass branch still goes on to consume the energy of the fault port, and the current limiting branch is still charging for capacitor C_1 . At $t=2.010$ s (t_8 moment), each branch current becomes 0A, the circuit breaker completes action.

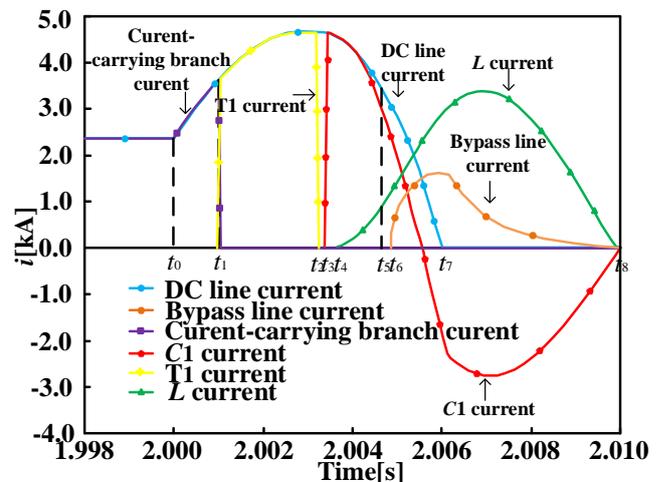


Fig. 11 Simulation waveform.

V. PERFORMANCE COMPARISON

To clearly analyze the breaking trait of this proposed direct current circuit breaker, the simulation results of the proposed direct current circuit breaker are compared with other schemes. Scheme I is a conventional hybrid DCCB of ABB company [22], scheme II is a hybrid high voltage direct current circuit breaker with current limitation [23], scheme III is the proposed capacitor-commutated current-limited hybrid DC circuit breaker, and the obtained simulation results are overall, syllabify and clarity shown in Fig. 12.

From Fig. 12, some results can be found.:

(1) The fault current value of Scheme I is the highest among the three schemes, reaching approximately 8.4kA, that is mainly due to the lack of a current-limiting circuit in its topology, which causes the fault current to rise rapidly to its

peak value, and it also has a longer breaking time.

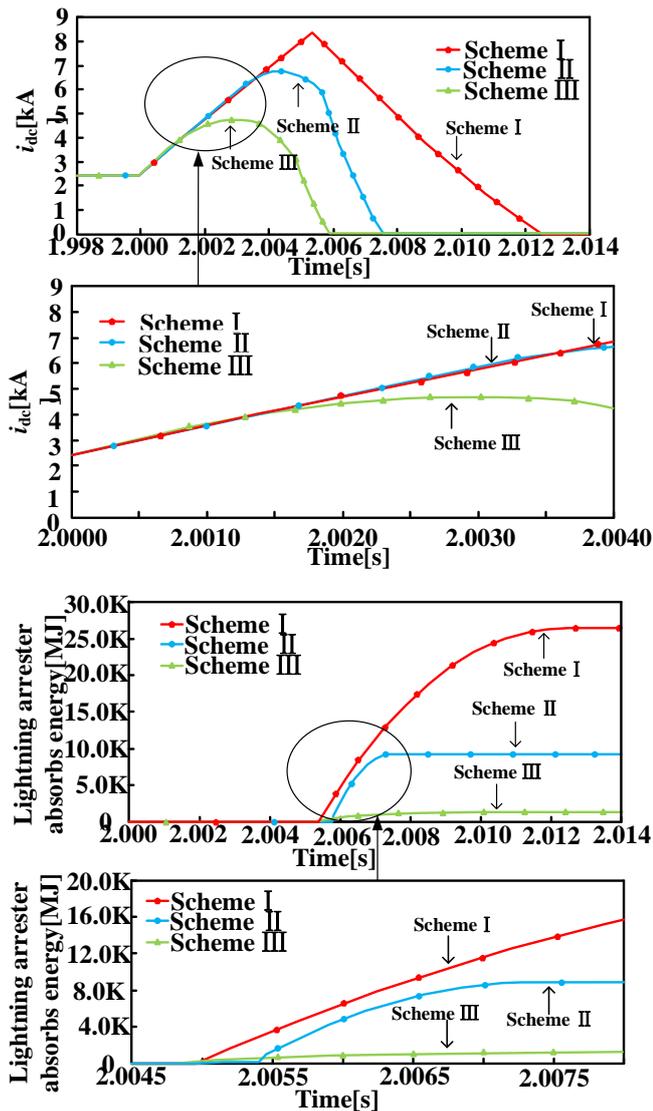


Fig. 12 Schemes comparison.

(2) In scheme II, a current-limiting part has a significant inhibitory influence on the fault current rise, and reduces the energy absorbed by lightning arrester, and a good economic performance of the equipment is promoted. Due to the inability to efficaciously control the fault current, although the shutdown time is shortened to 7.5ms, the fault current rapidly increases and quickly reaches the peak value before the arrester is triggered, fault elimination time is longer than scheme III.

(3) In scheme III, the current limiting section can provide significant suppression to the fault current, and the capacitors replaces the traditional structure of the IGBT to promote the economy of this proposed circuit breaker, on top of that, by adding a bypass branch, the energy absorbed by the working and normal lightning surge arrester is reduced, and some requirements of the surge arrester are lowered.

(4) The reduction of the peak current for Scheme III compared to Scheme I is 43.61%, the reduction of the peak current for Scheme III compared to Scheme II is 29.77%. These energy absorbed through the lightning arrester from Scheme III was reduced by 95.20% compared to the scheme I and 86.40% compared to the scheme II. In summary, the proposed scheme has very positive significance for the

development of DC circuit breakers.

(5) When the device specifications of each scheme are selected equally, an economic comparison is performed. The IGBT manifold in the through flow branch needs to withstand a voltage of 490 kV, after calculation, 108 IGBTs and 1 UFMS are required. The T1 thyristor group in the current limiting branch can take on a voltage of 500kV and has through-current capacity of 4.7kA. T3 thyristor manifold needs to withstand a voltage of 500kV and has through current capacity of 2.3kA. The T2 thyristor manifold has a through current capacity of 4.7kA at 810kV voltage value. Thyristor manifolds in the bypass branch need to withstand a voltage 434 kV and has a through-current capacity of 2.3 kA. The thyristor manifold in the cut-off branch has a throughput capacity of 16 kA at 900 kV voltage. In summary, after calculation, so 845 thyristors are required. The scheme III requires 530 diodes distributed over the bridge circuit and 180 diodes in the resistive inductive branch and capacitor C1 forming the loop, so the required diodes numbers are 710. Then, 1 UFMS, 108 IGBTs, 845 thyristors, and 710 diodes are required for the scheme III.

The number of devices required for the scheme I, the scheme II and the scheme III is shown in Table II.

TABLE II
COMPARISON RESULTS OF THE THREE PROGRAMS

Items	Scheme I	Scheme II	Scheme III
Number of IGBTs	1424	884	108
Number of Thyristors	0	627	845
Number of diodes	10	0	710
Number of capacitors	0	1	2

Due to the high price of IGBT, the price of one IGBT is roughly estimated about five times that of a thyristor, the price of one IGBT is roughly estimated about ten times that of a diode. The total cost of IGBT at high voltage levels is three times the total cost of capacitors. When IGBT in a large number of series-parallel connection need to consider the device current and voltage equalization problem, which may cause some IGBT to burn out [24]. Table II shows that the scheme III greatly reduces the number of IGBTs by contrast the other schemes I, II. Moreover, the correlative technology of thyristor is more mature than IGBT, and it is easier to deal with series-parallel connection problem of thyristor than IGBT under the same working condition. Therefore the scheme III is more economical than the other two schemes.

VI. CONCLUSION

In the paper, a new capacitor-commutated current-limited hybrid DC circuit breaker topology is proposed. Right after, the operational flow and principles of the topology have been analyzed. The system parameters are designed and analyzed in detail. Finally, the simulation is verified in four-ended system and compared with other schemes, the conclusion is as follows:

(1) The current limiting section is utilized to reduce the fault current peak and has good current limiting capability. The drop in current peak was reduced to about 43.61%, the charging and discharging circuit formed by the capacitor and the resistive inductive branch that can make it possible to

operate the capacitor infinitely by completing the charging only once.

(2) By the current-limiting inductor during the breaking phase of the hybrid DC circuit breaker, the breaking time of the fault is reduced, the fault breaking time reached 5.8ms.

(3) By replacing a portion of the IGBT branch with the capacitor, the device current and voltage equalization problem due to the series-parallel connection of IGBT is reduced. Then, these technical requirements and engineering difficulties about the hybrid DC circuit breaker are reduced, the IGBT failure rates is also reduced, and the economic benefit of the hybrid DC circuit breaker is improved.

(4) During the breaking phase of the hybrid DC circuit breaker, the fault-side inductance is bypassed through bypass branch, which reduces the energy absorption pressure on the lightning arrester, the absorbed energy by the lightning arrester has a reduction of 95.20%.

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