Tackling Differential Phase Shift Peaking and Degradation of Liquid Crystal Integrated Delay Line Phase Shifters with Barrel Plated Shut Micro-vias Across 1 GHz to 67 GHz

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***Abstract*—Liquid crystal (LC)-loaded reconfigurable passive wideband transmission line components (e.g., phase shifters) have found a home in feeding laboratory-grade phased array beam steering research that is not stringently requiring the system footprint and tuning speed. To widen their commercial application landscape, using vias for multi-layer components' integration into the system in low loss and reduced footprint is highly desirable. However, in wave-guiding circuits operating at millimeter-wave to optical frequencies, vias introduce a significant source of non-uniformity in liquid crystal-based devices. This study identifies a newly observed perturbation in the differential phase shift (DPS), adding to the previously reported surge in insertion loss caused by via-related effects. Two designs of LC-based phase shifters of an identical inverted microstrip-typed LC-accommodating structure but with diverse heights of barrel-plated filled vias (0.787 mm vs. 0.127 mm) are numerically compared across 1 GHz to 67 GHz. With the same LC-tunable length, the reduction of vias' height not only yields a compact solution but also enhances the DPS by 30% (featuring suppressed peaking and enhanced linearity), reduces the return loss by 11%, and mitigates the radiation loss by 24%. These findings highlight the critical need for advanced design and optimization strategies to mitigate the adverse electromagnetic impacts of micro vias, thereby preserving the performance and reliability of LC-based phase-modulating components for bandwidth-intensive 5G-and-beyond networks.**

***Index Terms*—filled vias, insertion loss, liquid crystal, micro vias, millimeter-wave, phase shifter, plated shut vias, vias**

I. Introduction

VIAS [1–16] are essential parts in radio frequency integrated circuits (RFIC), chiefly by interconnecting both sides of one substrate or multiple boards electrically. For the ever-evolving landscape of integrated sensing and communication realized by sophisticated phased array antenna beamforming architectures, vias play a rapidly expanding role in linking the phase shifting networks with the radiating elements with a minimum footprint. While the parasitic effects of introducing vias have been well documented in various setups of monolithic microwave integrated circuits (MMIC) [17–19], their impact on liquid crystals (LCs) based reconfigurable devices [20–22] have yet to be sufficiently clear. Particularly, the impacts of various types of vias, e.g., plated-through-holes vias (PTHV), and filled vias (FVs, otherwise knowns as plated shut) on LC phase-only components, e.g., phase shifters [23–27] for radio frequencies, and liquid crystal on silicon (LCOS) [28] for optical frequencies, are poorly understood.

In recognition for the pressing need of reducing both the power consumption and the device footprint in 5G-and-beyond networks, how to address the LC driving efficiently through multi-layer integration with control electronics using right-sized vias (in place of the power-hungry magnets driving [29][30]) is arguably tipping the balance. Without loss of generality, the benefits of FV over PTHV for LC-filled multi-layer devices are pictured in Fig. 1.

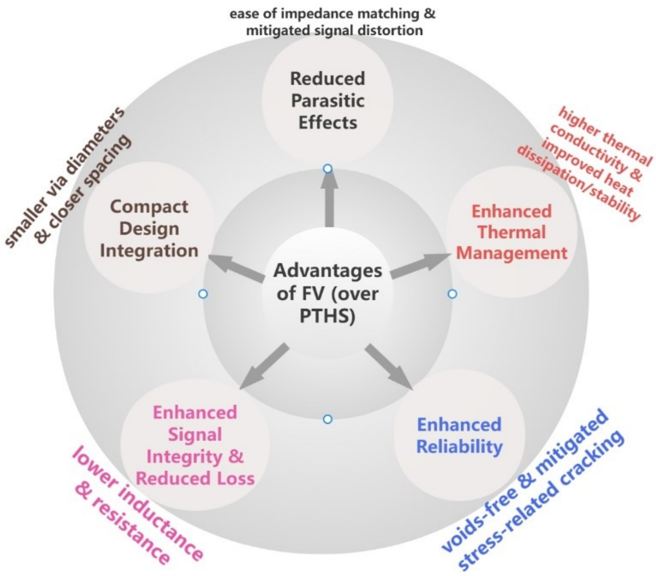

Fig. 1. Advantages of filled vias (FVs) over plated-through-hole vias (PTHVs) in liquid crystal (LC)-based multi-layer reconfigurable devices for millimeter-wave (mmW) and terahertz (THz) applications.

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Our simulation works on LC-filled multi-layer printed circuit board (PCB) devices with vias for vertical interconnections [31] have preliminarily quantified the escalation of insertion loss (IL) caused by vias and analyzed the dissipative power distribution across different loss elements in conductors and dielectrics. Furthermore, our experimental work reported at IEEE EPS 21st International Conference on Electronic Packaging Technology (ICEPT) [32] has investigated the vias' usage scenario for routing mixed signals (10 GHz and low-frequency biasing signals across layers of the circuit) in an LC-based phase shifter tightly integrated with bias tees. However, the impact of vias on another critical performance metric—differential phase shift (DPS)—has largely been overlooked. While some aspects of the research question concerning FVs in LC phase shifters have been embarked on from [32] at the lower-frequency X band, significant gaps remain in higher-frequency mmW (e.g., 67 GHz [33]) to fully understand the impact.

To address this, the present study investigates the phase modulation effects associated with varying sizes of FVs embedded within LC-filled reconfigurable delay line designs. For the LC-tuning structure, an inverted microstrip (IMS) topology is employed as the transmission line configuration to suppress parasitic propagation modes, such as coplanar strip line modes, which are prone to occur at mmW frequencies as illustrated in [34][35]. Fig. 2 presents a cross-sectional view of the input (or output) terminal, excluding the depiction of the 1.85 mm connector for clarity. The nematic LC molecules are electronically biased at a saturated voltage state (10 V as per the experimental outcome in [34]), so that the directors of the molecules are in line with the mmW polarization for maximum dipole moment (and hence the maximum permittivity macroscopically). The input and output terminals are implemented using top-launch patch circuits that form microstrip (MS) structures (no LC regions), resulting in a composite transmission topology characterized by a microstrip-to-inverted microstrip-to-microstrip (MS-IMS-MS) mode transition, as visualized in Figs. 3 and 4. Note that barrel plating is used for the FV (instead of pattern plating) to maintain the planarization with the top launch in 0.5 oz/ft², i.e., 17.5 μm.

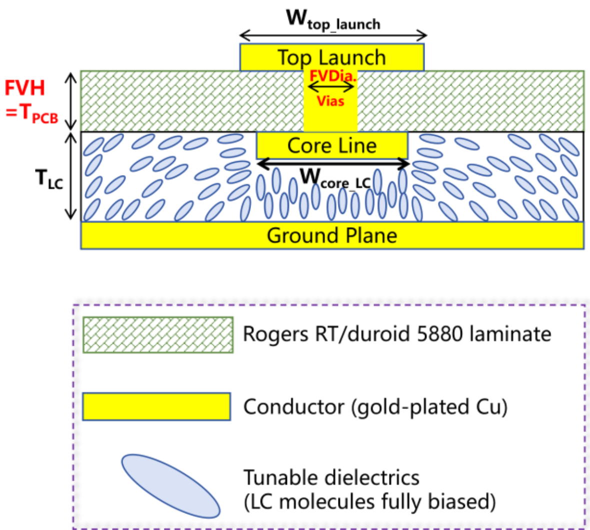

Fig. 2. Cross-sectional view of the LC-filled IMS delay line phase shifter's input (or output) terminal. LCs are biased at a saturated voltage state in this diagram to illustrate the dynamically tunable dipole moment of LCs.

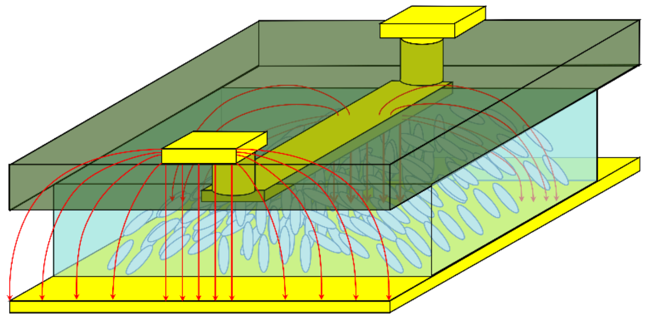

Fig. 3. Modes illustration for the MS-IMS-MS transition in the double-sided PCB of LC-filled IMS delay line phase shifter (with LCs biased at a saturated voltage state).

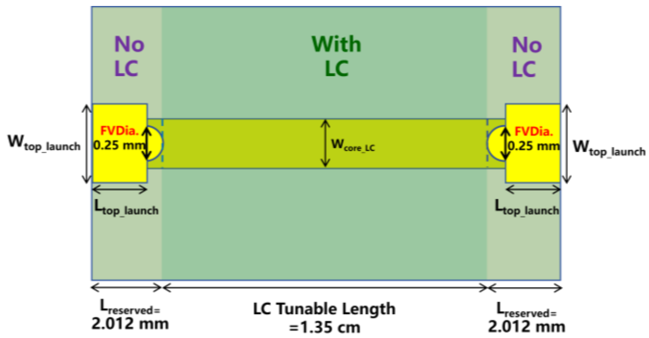

Fig. 4. Top view of the MS-IMS-MS topology and metalwork traces, highlighting tunable region with LC and non-tunable regions without LCs.

The top-launch metalized components are designed to interface with a pair of 1.85 mm connectors at both ends. While these connectors are not explicitly depicted in the schematics of Figs. 2–4 to maintain generality, their standard-sized pins are included in the simulations. Specifically, the parasitic effects of the connector pins are accounted for in the three-dimensional modeling and full-wave simulations conducted in this study, ensuring the results accurately reflect real-world performance.

Although the primary focus of this work is the numerical investigation of via-induced impacts on differential phase shift (DPS), readers interested in the detailed manufacturing and assembly techniques underpinning the LC-filled phase shifters explored here are encouraged to consult our previous publications [23][25][34]. These prior works detail iterative optimizations in the design, fabrication, and assembly processes, offering comprehensive insights into the practical implementation of LC-based phase shifters. By integrating these optimized techniques, this study extends their application to a rigorous examination of the electromagnetic effects of via structures, contributing to the broader understanding of LC-filled device design and performance.

II. Phase Shifting Peaking Due to Vias

When the thickness of the PCB substrate containing the vias approaches one-quarter of the effective or guided wavelength, it can lead to undesirable propagation of transverse electric modes, which complicates the electromagnetic behavior within the system. To illustrate this phenomenon (more specifically, the peaking or degradation in DPS and insertion loss), the height of the filled vias (FVH) in the PCB substrate is deliberately chosen to be one-quarter of the guided wavelength at 60 GHz. For this frequency, the quarter guided wavelength in the LC delay line part corresponds to FVH of 0.787 mm, a value that conveniently aligns with the standard laminate thickness (0.031 inch) of commercially available RT/duroid 5880 PTFE composites reinforced with glass microfibers material, featuring a low dielectric constant of 2.2±0.02 [36]). The impedance matching is specifically designed for the biased state of 0 V, where the LC director field aligns with the core transmission line (or millimeter-wave propagation direction) as depicted in Fig. 5. To ensure reliable signal transmission and measurement, 1.85 mm coaxial connectors are utilized.

The results presented in this, and subsequent sections are based on the geometry detailed in Table I, as well as the configurations shown in Figs. 5 and 6. These findings emphasize the influence of PCB substrate thickness (equivalent to the fixed via height, FVH) on overall device performance across the 1 GHz to 67 GHz frequency range. The impact is illustrated in Figs. 7–9 for differential phase shift (DPS), insertion loss (IL), and return loss (RL), respectively, under the two extreme LC biasing states (0 V and 10 V). The DPS results are derived by computing the phase shift difference between the 0 V bias state (Fig. 5) and the 10 V bias state (Fig. 6). This difference arises from the variation in wave propagation speed between these two extreme tuning states, driven by the controlled perturbation of LC permittivity under biasing. These findings provide key insights into the performance characteristics of the LC-loaded device under varying operational conditions.

TABLE I. KEY SIZES OF MS-IMS-MS INTERFACE IN THIS WORK.

This Work	MS-IMS-MS Topology		
	FV's diameter (FVDia.)	LC tunable length	$L_{reserved}$
Key sizes	0.25 mm	1.35 cm	2.012 mm

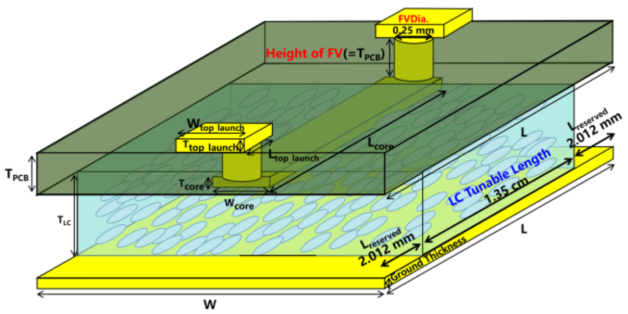

Fig. 5. Perspective view and size denotation of the LC-filled delay line phase shifter in an MS-IMS-MS topology, with LCs biased at 0 V state (permittivity=2.5, loss tangent=0.0123) as the impedance matching baseline.

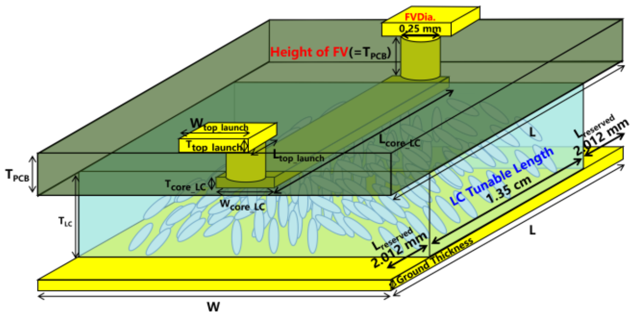

Fig. 6. Same geometry as Fig. 5 but with LCs biased at a saturated voltage state (10 V), i.e., permittivity=3.3, loss tangent=0.0032.

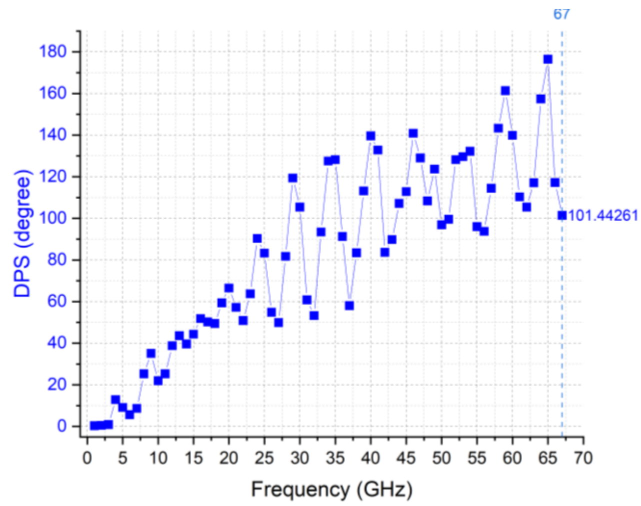

Fig. 7. DPS numerically characterized up to 67 GHz for the LC-filled delay line phase shifter in an MS-IMS-MS topology with FVH=0.787 mm.

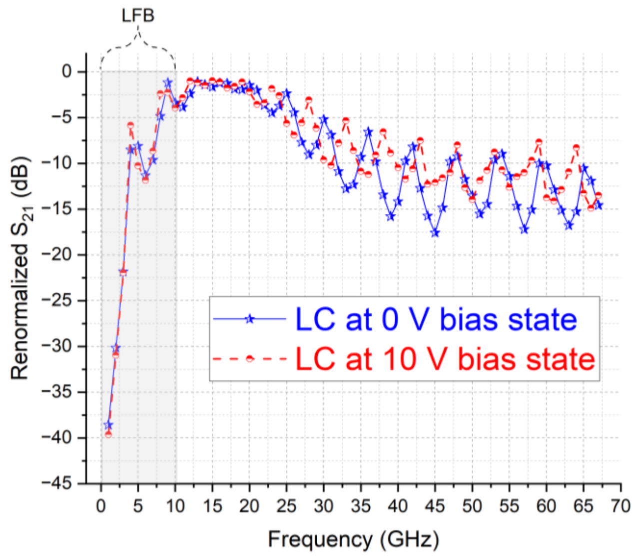

Fig. 8. IL numerically characterized up to 67 GHz for the LC-filled delay line phase shifter in an MS-IMS-MS topology with FVH=0.787 mm.

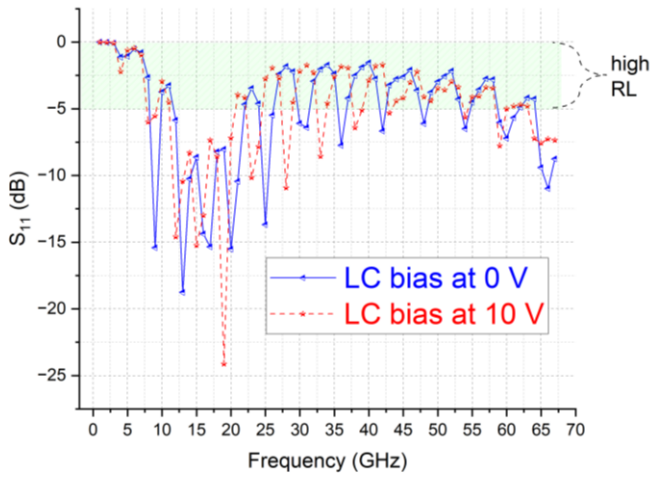

Fig. 9. RL numerically characterized up to 67 GHz for the LC-filled delay line phase shifter in an MS-IMS-MS topology with FVH=0.787 mm.

Based on the results presented in Figs. 7–9, the introduction of FVs with a height of one-quarter of the guided wavelength appears to significantly distort signal integrity and impede the broadband operation of the LC-filled delay line phase shifter. This degradation manifests in two distinct ways. In the phase domain, undesirable peaks in the DPS versus frequency (1 GHz to 67 GHz) are particularly evident in Fig. 6, with pronounced effects observed in the range of 20 GHz to 67 GHz. In the amplitude domain, a notable low-frequency breakdown (LFB) phenomenon is observed between 1 GHz and 10 GHz (denoted in Fig. 8). This is characterized by an unacceptably high return loss (RL, with S11 exceeding –5 dB as denoted in Fig. 9) and severe insertion loss (S21 ranging from −40 dB to −10 dB in Fig. 8 for the LFB regime).

III. Mitigating Vias' Impacts

To address the issues of DPS peaking and IL surges, two designs of the LC-filled multilayer integrated delay line phase shifter with barrel-plated shut micro vias are proposed and evaluated in full-wave simulations. These designs differ in the height of the FVHs and, consequently, the thickness of the PCB substrate, which are 0.787 mm and 0.127 mm, respectively (Figs. 10–13). The thickness of the PCB is found to have a significant impact on the device's performance.

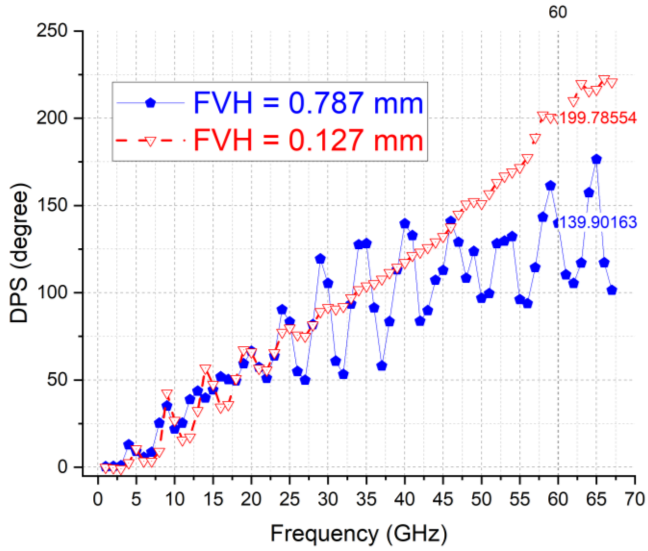

Fig. 10. DPS comparison across 1 GHz to 67 GHz between two designs of diverse FVHs for the LC-filled delay line phase shifter in an MS-IMS-MS topology.

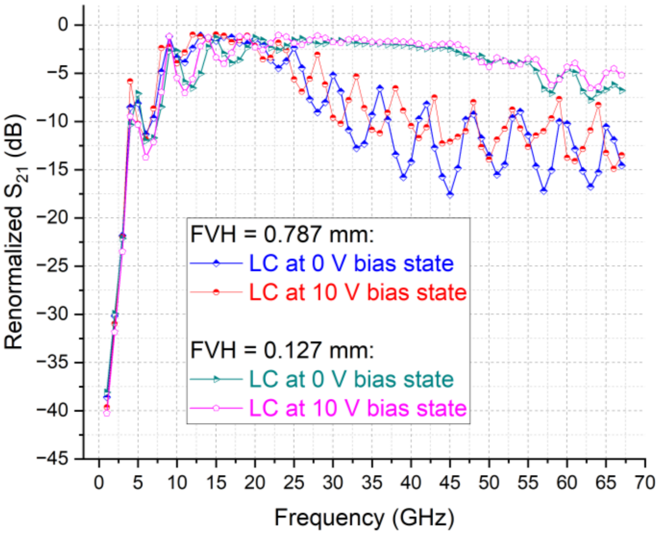

Fig. 11. IL comparison across 1 GHz to 67 GHz between two designs of diverse FVHs for the LC-filled delay line phase shifter in an MS-IMS-MS topology.

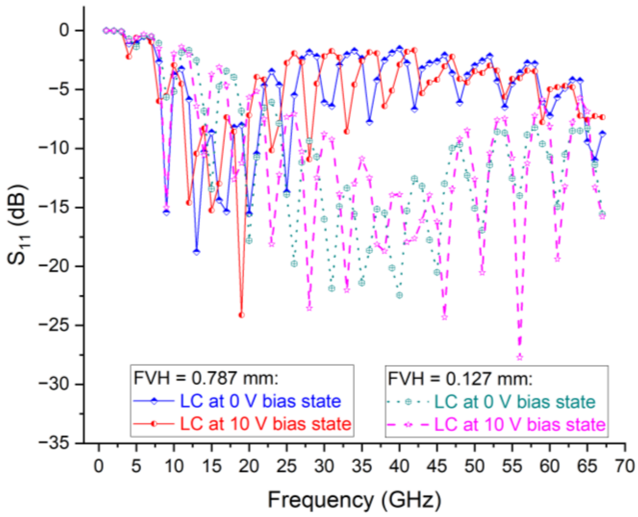

Fig. 12. RL comparison across 1 GHz to 67 GHz between two designs of diverse FVHs for the LC-filled delay line phase shifter in an MS-IMS-MS topology.

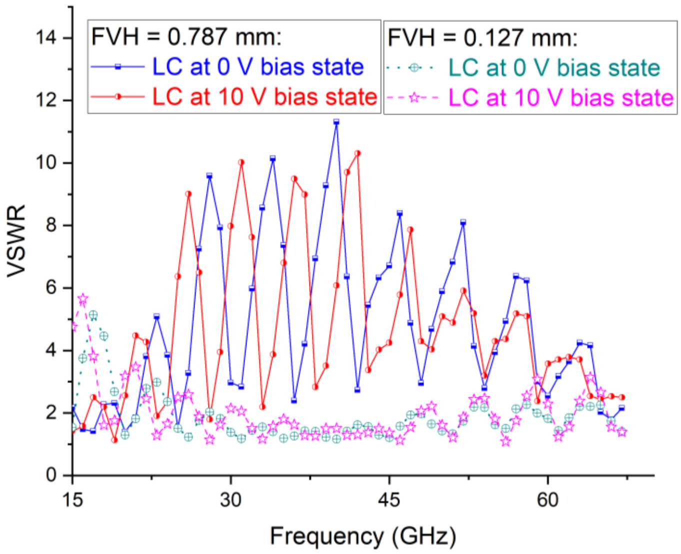

Fig. 13. VSWR (voltage standing wave ratio) comparison up to 67 GHz between two designs of diverse FVHs for the LC-filled delay line phase shifter in an MS-IMS-MS topology.

The results pictured in Figs. 10–13 are information-rich for designing phase shifters suitable for bandwidth-intensive applications. As shown in Fig. 10, the DPS peaking issue observed in the design with FVH of 0.787 mm has been significantly mitigated by reducing the FVH to 0.127 mm. This adjustment corresponds to an alternative commercially available PCB thickness, which addresses the challenges associated with the 0.787 mm design, including resonance, impedance mismatching, unwanted coupling, and radiation.

The mitigation of DPS peaking and enhancement of linearity are notably more pronounced above 30 GHz compared to lower frequencies. For frequencies below 25 GHz, the guided wavelength exceeds 7.6 mm, while the FVH is 0.787 mm—less than one-tenth of the guided wavelength. In this frequency range, reducing the FVH results in only minor changes in DPS, as evidenced by the two DPS curves showing substantial agreement in both magnitude and trend below 25 GHz.

At frequencies above 25 GHz, the guided wavelength decreases, necessitating shorter vias to minimize the discontinuity through which the signal propagates. At 60

GHz, where the guided wavelength is 3.16 mm, an FVH of 0.787 mm corresponds to one-quarter of the guided wavelength, whereas a reduced FVH of 0.127 mm corresponds to 1/25 of the guided wavelength. This reduction significantly mitigates the discontinuity effects introduced by the vias. Specifically, at 60 GHz, these discontinuity effects lead to a 30% reduction in phase shift (from 199° to 139°, assuming the same LC tunable length), a 9% decrease in material absorption (primarily due to a reduced wave-occupying volume in the LC), an 11% increase in return loss (RL), and a 24% increase in radiation.

The findings also provide guidance for cost-effective future designs. From a material perspective, the design with an FVH of 0.787 mm incurs higher costs due to the greater amount of filler conducting material (e.g., gold) required compared to the thinner 0.127 mm design. Additionally, optimal via dimensions can be derived from the currently conservative filled vias configuration analyzed in this study. By eliminating excess (wasted) space—such as the inaccessible inner portions of metalized vias due to the skin effect [37][38]—designs can further reduce costs, particularly for applications where thermal conductivity is not a critical requirement.

IV. Results Discussions and Future Work

A. *Validation using Time-domain Reflectometry*

Liquid crystal (LC)-loaded, reconfigurable wideband transmission line components, such as phase shifters, have been widely employed in laboratory-grade phased array beam steering research, particularly in scenarios where system footprint and tuning speed are not critical constraints. To transition these devices toward commercial applications, there was broad agreement that achieving cost-effective, low-loss, and compact integration within systems is paramount. However, in wave-guiding circuits operating at millimeter-wave to optical frequencies, the inclusion of vias introduces additional sources of non-uniformity in LC-based devices. This study highlights these challenges, as evidenced by via-induced perturbations in differential phase shift—an effect well-documented in conventional PCB circuits but underexplored in LC-integrated systems.

This investigation in the frequency domain examines the electromagnetic impact of via heights on LC-loaded passive planar transmission lines with top-launch microstrip access, operating up to 67 GHz. The results reveal that deviations from the desired mono-mode transverse electromagnetic (TEM) operation adversely affect both the phase-shifting performance and the dissipative loss characteristics of the devices. These findings emphasize the necessity of optimizing via dimensions to preserve the intended electromagnetic behavior in high-frequency applications.

Notably, the results presented in this work are derived from full-wave simulations conducted using the High-Frequency Structure Simulator (HFSS) in the frequency domain (FD). For computational validation, time-domain techniques, such as time-domain reflectometry (TDR), could be employed (potentially using the same or alternative software) for cross-benchmarking purposes. While the FD approach effectively characterizes the overall transmitted and reflected responses, it does not provide spatial or temporal localization of discontinuities within the structure. In contrast, the TDR method addresses this limitation by precisely identifying problematic locations in the metalwork traces that lead to reflections. For example, while the FD approach examines the relationship between the millimeter-wave (mmW) guided wavelength and the electrical length of the vias, the TDR method evaluates the signal rise time and the time delay introduced by the micro vias, offering a complementary perspective.

B. *In-depth Interpretation based on Aspect Ratios*

Future study will focus on developing innovative strategies to minimize via-induced non-uniformities, thereby facilitating the practical deployment of LC-loaded devices in high-frequency systems with stringent performance requirements. Specifically, the aspect ratio (AR) of the filled vias' height (FVH) to vias' diameter (FVDia.), as per (1), will be studied to comprehensively assess its impact on device performance (i.e., quantifying DPS vs. AR, IL vs. AR at a targeting frequency of interest).

$$AR = FVH/FVDia. \tag{1}$$

Strategic AR adjustments, informed by both electromagnetic and mechanical considerations, can responsibly enhance the device's reliability and functionality. Electromagnetically, a higher AR (taller vias relative to their diameter, as depicted in Fig. 14) increases the discontinuity in the transmission path, causing greater impedance mismatch. This can lead to higher return loss and insertion loss, particularly at higher frequencies where the wavelength is smaller, making these discontinuities more pronounced. A lower AR (shorter FVH relative to FVDia.) is preferable for minimizing parasitic effects and improving electromagnetic performance. Reducing FVH while slightly increasing FVDia. can achieve a favorable compromise for most applications. However, excessively large FVDia. can increase the capacitance of the vias, which must also be optimized for impedance matching.

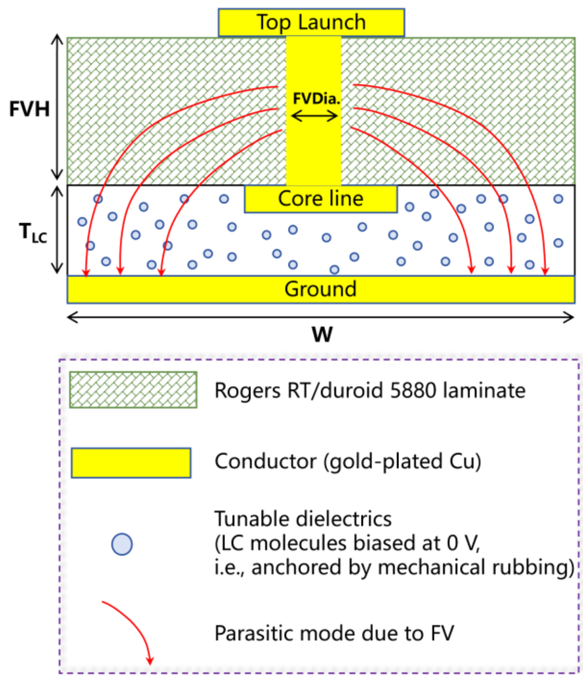

Fig. 14. Parasitic mode illustration (cross-sectional view) for the LC-filled delay line phase shifter, featuring FVs with high AR (tall FVH).

From the lens of LC-driving and DPS's linearity, as the AR increases, the perturbation in the electric field near the vias becomes significant (actioning on both the mmW signal and the low-frequency biasing field), leading to non-uniformities in the LC alignment (biasing-field dependent). This can reduce the linearity of DPS and introduce undesirable peaking effects at specific frequencies, as evidenced in Fig. 7 (and remediated in Fig. 10 by reducing the AR with a shorter FVH).

Taller vias with a high AR act as unintended radiating structures (see Fig. 14), especially at mmW frequencies, increasing radiation loss. Lowering the AR reduces the effective length of the radiating structure relative to the wavelength.

Mechanically, high AR vias are challenging to fill reliably during manufacturing due to limitations in via plating or filling processes. Voids or uneven fillings can introduce parasitic effects and reduce the mechanical integrity of the vias. Reducing the AR improves manufacturability by enabling uniform metal deposition. Typical manufacturing processes impose limits on AR, as is customary, often with a maximum AR of around 8:1 to 10:1 [39][40] for standard PCB fabrication techniques. ARs exceeding this range may require advanced techniques, e.g., laser drilling [41] or specialized plating methods, which increase costs. Taller vias (high AR) are more prone to mechanical stress, especially during temperature cycling. This can lead to cracks [42] or delamination at the via-substrate interface, compromising device reliability.

In addition to the AR of the FV itself as per (1), there is another AR-related possibility of optimization based on the ratio of the FVH to the LC thickness (TLC), which may also tip the balance in the signal integrity and DPS linearity. The depiction in Fig. 15 (low FVH/TLC ratio) gives an exemplary illustration of the sparsely distributed parasitic mode (smearing) as compared with the tightly coupled case shown in Fig. 14 (higher FVH/TLC ratio).

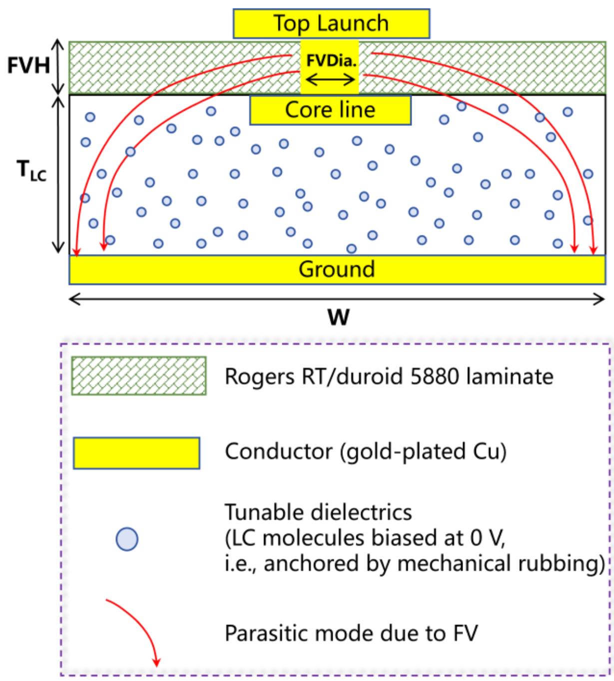

Fig. 15. Illustration of parasitic mode smearing for thick LC and short FVH case for the LC-filled delay line phase shifter design (cross-sectional view).

Among the two fleets of architectures, what makes the design tradeoff (Fig. 15 vs. Fig. 14) an especially onerous challenge is the tuning response time (RT), which is quadratically dependent on the LC thickness (TLC) as per (2). It is important to note that (2) applies to both the turning-on and turning-off operations. Specifically, it represents the settling time associated with voltage enforcement during activation and voltage removal during deactivation (relaxation), capturing the transient response in both cases. While the smearing of the parasitic mode (Fig. 15) by a large TLC is envisaged to aid in suppressing the undesirable peaking and non-linearity of DPS, the tuning speed (response time) raises a new alarm for device designers to address.

As an illustrative example, the response time (RT) is evaluated for three cases with LC thicknesses of 140 µm, 40 µm, and 4 µm, while maintaining the same LC material type (nematic) and grade (GT3-24002). Given the identical viscoelastic behavior of the LC material under the same voltage stimuli, the recorded response time (RT) values are analyzed and compared, corresponding to the representative cases illustrated in Figs. 15 and 14, respectively. The observed switching dynamics, however, remain significantly slower than those of conventional semiconductor-based phase shifters, which dominate mainstream applications due to their superior speed.

To address this limitation, the analysis extends to a prospective prototype designed with an ultra-thin LC layer (4 µm), aiming for switching-off and switching-on times of approximately 9 milliseconds and 8 milliseconds, respectively. This level of performance marks a step toward achieving switching speeds that are more competitive with alternative phase-shifting technologies.

$$RT \propto TLC^2 \quad (2)$$

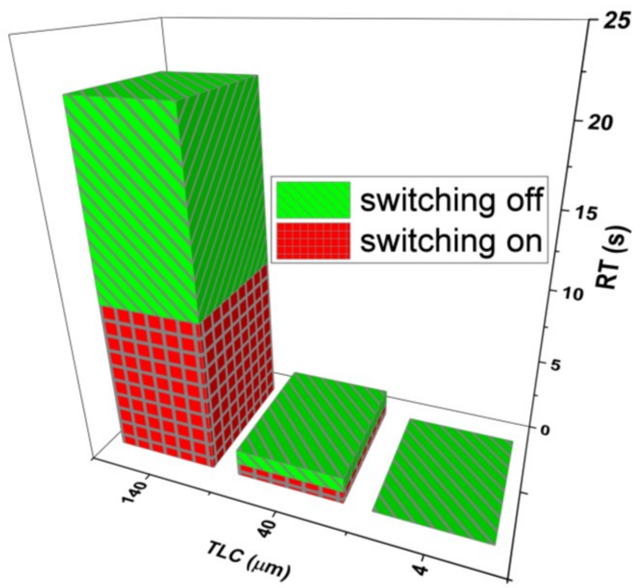

Fig. 16. Illustration of response time (RT) comparison, specifically switching-on and switching-off times, between a thick LC (140 µm) and a short FVH case in the LC-filled delay line phase shifter design (Fig. 15) and FVs with high aspect ratio (tall FVH and thin LC of 40 µm, as shown in Fig. 14). A future prototype with an extremely thinner LC layer of 4 µm is illustrated.

The results presented in Fig. 16 are structured in a cumulative manner, where the switching-off and switching-on times are summed within a single column. This approach provides a comprehensive assessment of the overall tuning speed, facilitating a clearer comparison of the total response time across different cases.

In summary, understanding the multi-faceted technological intricacies and precisely engineering the micro vias help improve the design of future LC-embedded multilayer phase shifters at scale.

C. Potential of Hybrid and Heterogeneous Integration

Future efforts may embrace hybrid and heterogeneous integration techniques to address the identified challenges. These approaches will focus on seamlessly combining LC-based components (e.g., phase shifters as targeted in this work) with other advanced materials (e.g., graphene) and alternative device architectures (e.g., substrate integrated waveguides) to enhance overall system performance. By miniaturing and integrating LC-loaded devices with other high-performance materials, such as low-loss substrates or advanced interconnect technologies, it will be possible to further reduce parasitic effects, improve thermal stability, and minimize signal distortion across a wide frequency spectrum.

Furthermore, heterogeneous integration strategies will investigate novel packaging solutions, including wafer-level and chip-scale techniques, to achieve compact, lightweight, and robust designs suitable for practical deployment in phased antennas array. These methods will not only optimize the electrical and mechanical properties of LC-loaded devices but also enable their integration with complementary technologies, such as MEMS (micro-electromechanical systems) [43][44], photonics (for THz deployment), or advanced RF components, to extend their functionality without compromising affordability.

Beyond proof-of-concept trials, future research will emphasize the development of scalable fabrication techniques that adhere to industry standards, ensuring cost-effective production without compromising device reliability. Additionally, the investigation of multi-frequency and broadband operation, facilitated by these integration approaches, holds significant promise for broadening the application of LC-loaded components in emerging domains such as 6G communication [45][46], advanced radar systems [47][48], and terahertz (THz) sensing [49][50].

Overall, these inspiring updates and advancements are expected to significantly enhance the performance, scalability, and versatility of LC-loaded components [51–54], paving the way for their adoption in compact, efficient, and high-frequency systems across a diverse range of applications.

V. Conclusion

From 1 GHz to 67 GHz, this study numerically illustrates the significant impact of via height on the performance of liquid crystal (LC)-based phase shifters, particularly in terms of differential phase shift (DPS) and overall electromagnetic behavior. By comparing two phase shifter designs with varying via heights (0.787 mm vs. 0.127 mm), it was shown that reducing the via height not only leads to a more compact design but also improves key performance metrics, including a 30% enhancement in DPS, 11% reduction in return loss, and 24% reduction in radiation loss. These results imply the importance of advanced design strategies to mitigate the detrimental effects of micro vias, thus ensuring the efficiency and reliability of LC-based devices for future high-frequency applications, extending beyond the traditional display domain [55][56].

Through in-depth investigations from the lens of aspect ratios and response times, the findings offer valuable insights into the optimization of phase-modulating components within wave-guiding circuits. These results not only deepen the understanding of the interplay between structural parameters and device performance but also provide a foundation for improving the design of liquid crystal-based components. By addressing key challenges related to tuning speed, efficiency, and footprint reduction, the study paves the way for the enhanced commercial viability of these components, particularly in the context of high-frequency applications, e.g., 5G and beyond.

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