Design and Comparative Analysis of Vertical and Planar Tunnel Field Effect Transistors for Analog Performance Parameters

V.Saraswathi, N.Siddaiah

***Abstract*—This work introduces the design and comparative study of a new vertical Tunnel Field-Effect Transistor (TFET) structure with remarkable performance improvements over traditional planar TFETs. The new device combines a dual-gate architecture with heterostructure materials and multi-dielectric configurations to maximize tunneling efficiency, minimize threshold voltage, and increase drive current. Using simulation-based analysis, the vertical TFET exhibits a subthreshold swing (SS) of as low as 49 mV/decade, an I_{on}/I_{off} ratio of as high as 1.5×10^8 and better short-channel effect suppression. The impact of various dielectric materials—SiO_2, HfO_2, Si_3N_4, and their combinations—on device performance is comprehensively explored, revealing the trade-offs among leakage current, drive current, and switching efficiency. High-k dielectrics, especially $HfO_2 - Si_3N_4$ combinations, significantly improve the device performance by minimizing on-resistance and optimizing carrier transport characteristics. These improvements make the proposed vertical TFET a viable candidate for low-power and high-speed applications in next-generation nanoelectronics and ultra-low-power integrated circuits.**

***Index Terms*—TFET, MOSFET, subthreshold, short channel, tunneling**

I. Introduction

ONE such promising candidate among the novel device technologies is the Tunnel Field Effect Transistor, which puts itself forward as one of the future candidates to succeed the metal-oxide-semiconductor field-effect transistor for energy-efficient and high-speed integrated circuits [1]. TFETs exploit the quantum mechanical BTBT mechanism to overcome the Boltzmann tyranny of the conventional 60 mV/dec subthreshold swing barrier even at room temperature conditions (300 K). That makes TFETs ideal devices for low-power applications and advanced switching technologies [2].

However, a weakness of the BTBT mechanism is that it inherently restricts the drive current (I_{on}) to much smaller values than what can be achieved by classical MOSFETs [3]. To address this, ongoing research focuses on optimizing various aspects of TFET design, including the choice of semiconductor materials, gate dielectrics, and source, channel, and drain doping profiles [4]-[6]. Considerations such as device architecture, the influence of trap charges, and temperature effects are also being rigorously explored. These include the improvement of performance, reliability, and exploitation of all the advantages TFETs have for energy-efficient digital and analog applications in the next generation of electronics [7]-[10].

Scaling transistors down in dimensions and supply voltages has always been a very effective way of lowering power dissipation in electronic circuits. As MOSFETs are scaled down to nanometer dimensions, physical limitations start to appear mainly because of the short-channel effects [11]. These degrade device performance by raising off-state current and reducing drive current. Both these are undesirable aspects of efficient operation.

Low off-state current is the requirement for maintaining a minimal subthreshold swing at room temperature. In traditional FETs, the SS is, however, fundamentally restricted to 60 mV/decade because of the thermionic emission mechanism by which it generates current [12]. Since this mechanism intrinsically depends on temperature, the conventional FET can hardly achieve a good subthreshold performance that can adequately meet the needs of modern low-power applications [13]. This limitation underlines the need for innovation in new device architectures such as TFETs that can break through these limitations and offer better performance [14]-[19].

Researchers are actively exploring alternative device technologies to meet the requirements of future electronics, overcoming the inherent disadvantages of MOSFETs. Of these, TFETs could become one of the most promising candidates due to some unique advantages. Utilizing band-to-band tunneling instead of conventional thermionic emission, TFETs show very low off-state currents and make it an excellent candidate for ultra-low-power application. This tunneling mechanism also allows TFETs to maintain subthreshold swing (SS) values below the fundamental limit of 60 mV/decade whereas in MOSFET it is not possible [20]. Therefore, TFET possesses substantially reduced leakage currents and is less sensitive to temperature fluctuations, making it a strong candidate for energy-efficient designs.

In a TFET, the control over BTBT process is served by gate since it controls the surface potential of channel with great accuracy and thus makes possible accurate switching properties. However, TFETs remain limited in terms of their on-state drive currents (I_{on}) because their BTBT efficiency is inherently limited. To overcome these limitations, researchers have incorporated heterostructure materials with bandgaps, smaller on the source side, within the device [21]. Incorporation of these materials limits the tunneling barrier, reduces V_t, and promotes the drive current. This approach optimizes the performance of TFETs by

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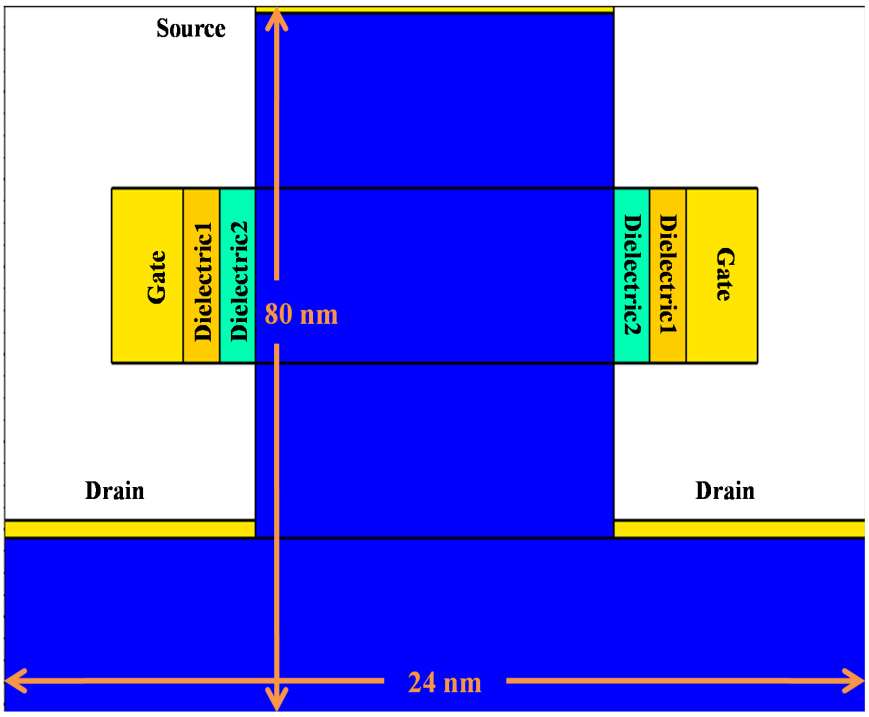


Fig. 1: Schematic representation of the proposed vertical TFET structure, highlighting the dual-gate configuration and optimized dielectric layers for enhanced tunneling efficiency

bridging the gap between the low power of its advantages and the high-performance demands of modern applications [22].

II. Structure of Proposed Device

A new vertical tunnel field-effect transistor (TFET) structure as shown in Figure 1, is designed carefully to optimize performance by advanced material and geometrical configurations. The multilayer architecture is incorporated, and the regions are defined carefully and meshed, ensuring accurate modeling in this device. High-quality materials, such as silicon and SiO_2, are utilized in order to take advantage of their desirable electronic properties for efficient tunneling and carrier transport. A specific region of the structure contains dopings that have a combination of p-type and n-type doping at different concentrations, thus providing strong p-n junction formation and availability of efficient tunneling mechanism, which is essential for TFET operation.

The gate electrodes are strategically placed and defined to effectively modulate the tunneling barrier. This dual-gate configuration features primary and secondary gate electrodes that couple with the silicon channel. This dual-gate design controls the tunneling current much better and suppresses the leakage pathways, thereby having improved subthreshold swing and enhanced device performance. Detailed contact definitions also provide accurate work function alignment, thus making possible the creation of sharp potential barriers tailored for tunneling.

For robust functionality of the structure, the model including non-local band-to-band tunneling, quantum tunneling parameters are incorporated in the simulation environment. Models such as Shockley-Read-Hall (SRH) recombination and carrier mobility models are advanced kinds that can ensure good behavior under a variety of operating conditions. Thus, by maintaining detailed meshing and material region definitions, the structure can effectively deal with the device challenges in making a minimal short-channel impact and enhancing on-current capabilities, thereby making this TFET an innovative approach to modern transistor design.

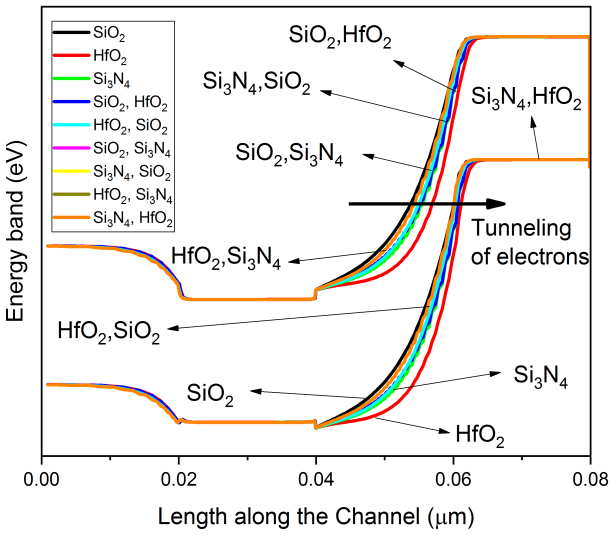


Fig. 2: Energy band diagram of the proposed TFET for different dielectric materials, illustrating variations in band alignment and tunneling barrier

This vertical TFET structure has an intricate meshing approach to simulate such critically important areas at

TABLE I: Impact of Dielectric Combination on Energy Band Alignment and Tunneling Barrier

Dielectric Material	Band Alignment Shift	Tunneling Barrier Reduction	Carrier Transport Efficiency	Short-Channel Effect Suppression
SiO_2	Minimal	High	Low	Moderate
HfO_2	Strong	Low	High	Strong
Si_3N_4	Moderate	Moderate	Moderate	Balanced
$HfO_2 - Si_3N_4$	Significant	Low	High	Strong
$SiO_2 - Si_3N_4$	Maximum	Very Low	Very High	Excellent

the highest of resolutions. In the horizontal and vertical directions, mesh densities are thus defined with care in terms of any electric field variations, potential distribution, and doping profiles. These parameters are of prime importance in evaluating quantum tunneling effects in the device and the overall electrostatic integrity of the device. Regions made of silicon and high-k dielectric materials are defined precisely to maximize the device's gate control while minimizing leakage currents, both factors helping in a reduced power dissipation compared to conventional transistors.

Advanced materials such as silicon dioxide (SiO_2) for dielectric layers ensure good gate insulation and stability in nanoscale dimensions. Dual-dielectric configuration along with having different materials on either end offers a tailored distribution of the electric field across the channel, providing enhanced tunneling probabilities along with a higher ratio of I_{on} to I_{off}. This approach also aids in interface state control, thus improving the reliability and long-term stability of operation of the device.

The symmetric arrangement of the dual-gate electrodes enhances control over the tunneling junction, and it provides improved energy efficiency and better parasitic suppression. The gates must work together in order to create a uniform electric field-optimal tunneling while maintaining high drive currents. Detailed definition of source, drain, and other contact electrodes results in a smooth flow of charge carriers across the device, focusing on minimizing series resistance and optimizing the pathways of current conduction.

All these phenomena are reflected by the application of nonlocal tunneling models with quantum corrections as shown in Figure 2 , where mass parameters for electrons and holes are considered during device performance simulation. Including these, the device is able to capture quantum tunneling behavior in detail, especially under varying gate biases. This advanced modeling ensures that the simulation closely mirrors real-world performance, making the proposed structure a significant step forward in the development of low-power, high-efficiency transistors for next-generation electronics. The impact of dielectrics on Energy band is shown in Table I.

III. Results & Discussion

A more in-depth analysis of the electrical properties of the introduced vertical TFET considering various dielectric material configurations is discussed. Each of the figures provides information on how the different dielectrics affect the performance of the device, starting from current modulation up to resistance behavior.

As presented in Figure 3, it shows that the $I_d - V_{gs}$ curve has been considered as the change in drain current with respect to different gate voltages for various dielectric materials. This plot illustrates the device's feature of current modulation by gate voltage, and materials like HfO_2 tend to present higher on-current values compared to SiO_2. The better current modulation in high-k dielectric material HfO_2, being responsible for its superior gating control, has reduced the tunneling barrier, which enhances the conduction of currents.

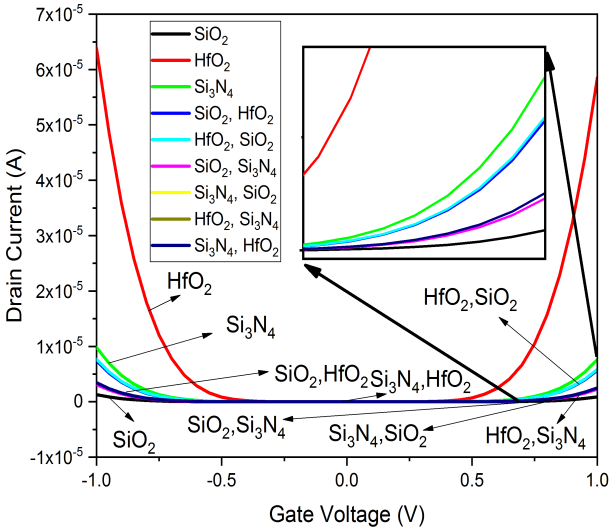


Fig. 3: Comparison of drain current characteristics for various dielectric configurations, highlighting the effect of high-k materials on gate control

Figure 4 plots $I_d - V_{gs}$ with a logarithmic scale, focusing attention on off-state leakage current and on/off current ratio of different materials. The logarithmic scale ensures that differences in leakage currents that are typically negligible become observable, and it does so in such a way that dielectric combinations like HfO_2-SiO_2 show a significant off-state current reduction accompanied by a high on-state current. The latter is vital for low-power technologies, for which leakage current suppression becomes the dominant goal.

In Figure 5, the gate voltage dependence of transconductance shows how dielectric materials affect the amplification of the device. Peak transconductance changes significantly with the dielectric used, and in comparison, HfO_2 and hybrid dielectric HfO_2-Si_3N_4 indicate superior characteristics. Therefore, high-k dielectrics yield a greater coupling efficiency while offering more control over channel conductivity, making the device even more sensitive to changes in the gate voltage.

Figure 6 $I_d - V_{ds}$ characteristics a plot of the variation of drain current with drain-source voltage for various dielectrics. The curves depict the linear and saturation regions in the operation of the TFET. High-k materials like HfO_2 exhibit higher saturation currents, which mean

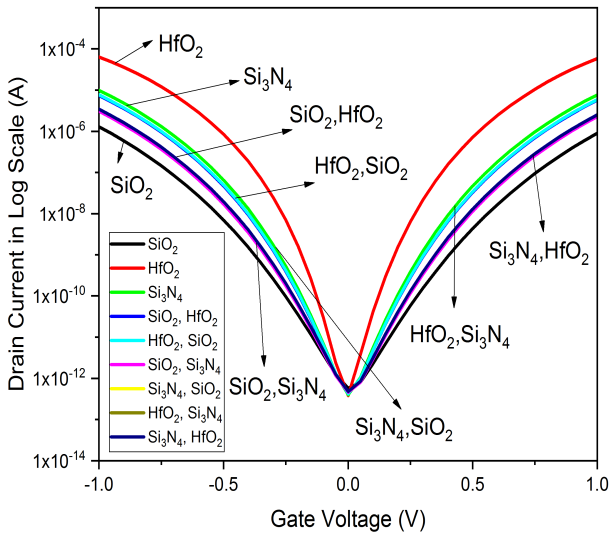


Fig. 4: Log-scale $I_d - V_{gs}$ characteristics for different dielectric materials, emphasizing the impact of dielectrics on off-state leakage current

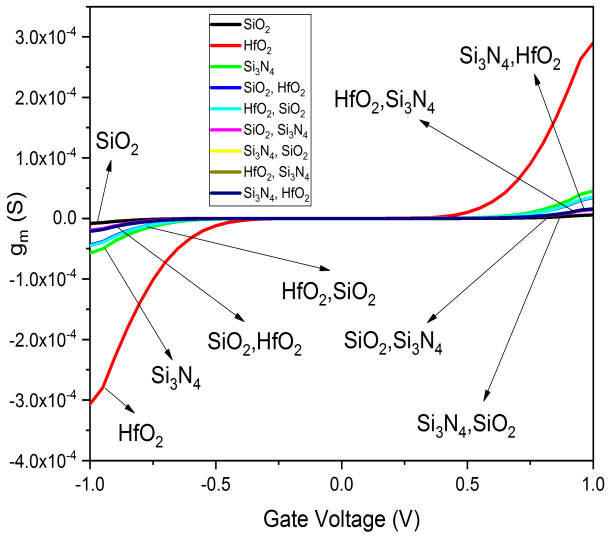


Fig. 5: Variation of Transconductance with Gate voltage for different dielectric materials

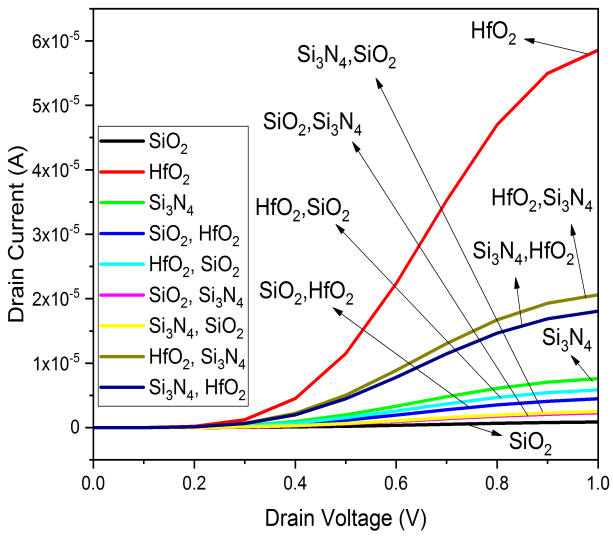


Fig. 6: $I_d - V_{ds}$ for different dielectric materials

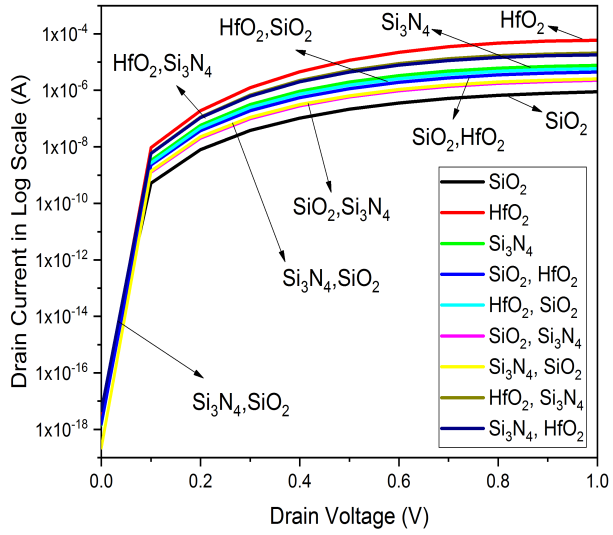


Fig. 7: $I_d - V_{ds}$ in Log scale for different dielectric materials

efficient carrier transport along with a smaller resistance in the channel. This implies that material selection should target to get larger drive currents for high-performance applications.

Figure 7 shows the logarithmic scale plot of $I_d - V_{ds}$, which reveals further differences in subthreshold behavior. The steep transitions from off-state to on-state current indicate dielectric materials have been able to successfully minimize the short-channel effects. Material combinations like HfO_2-SiO_2 display smoother transitions and a low subthreshold swings across different operational conditions, improving overall device reliability.

Figure 8 depicts the conductance versus gate voltage variation, which elucidates how the same device's conductive state depends on dielectric properties. The highest dielectric constant materials provide better gate coupling due to improved conductance characteristic. Therefore, optimizations on dielectric properties should balance between the power efficiency and performance in TFETs.

Finally, Figure 9 is a plot of on-resistance as a function of gate voltage, which is inversely proportional to the conductivity of the device in the on-state. In this regard, combinations of dielectrics such as HfO_2-Si_3N_4 yield lower on-resistances that correspond to lower power dissipation and improved efficiency. This plot indicates the advantage of high-k dielectrics to reduce resistive losses in the device.

The band-to-band tunneling recombination rates in different dielectric material configurations for the proposed TFET are shown in Figure 10 in terms of contour plots. It is clearly a visual map of where the recombination takes place and how strongly it happens in the device structure; these contours directly reflect the efficacy of tunneling and the role of dielectric materials to modulate this behavior. The combination of material results in a particular distribution of tunneling recombination, which is due to the difference in electric field intensity, band alignment, and different carrier transport mechanisms.

In Figure 10(a), the SiO_2 recombination contour shows a

TABLE II: Comparison of key electrical parameters of the proposed vertical TFET for different dielectric materials, including threshold voltage (V_t), subthreshold swing (SS), off-state current (I_{off}), on-state current (I_{on}), and I_{on}/I_{off} ratio

	V_t (V)	SS (mV/dec)	I_{off} (A)	I_{on} (A)	I_{on}/I_{off}
SiO_2	0.75	104	5.7×10^{-13}	8.9×10^{-7}	1.5×10^{6}
HfO_2	0.37	49	3.8×10^{-13}	5.8×10^{-5}	1.5×10^{8}
Si_3N_4	0.55	77	3.9×10^{-13}	7.6×10^{-6}	1.9×10^{7}
SiO_2, HfO_2	-0.57	74	4.18×10^{-13}	5.6×10^{-6}	1.36×10^{7}
HfO_2, SiO_2	-0.57	73	4.2×10^{-13}	5.8×10^{-6}	1.39×10^{7}
SiO_2, Si_3N_4	-0.67	88	4.58×10^{-13}	2.28×10^{-6}	4.9×10^{6}
Si_3N_4, SiO_2	-0.65	87	4.7×10^{-13}	2.5×10^{-6}	5.2×10^{6}
HfO_2, Si_3N_4	0.48	88	3.7×10^{-13}	1.7×10^{-5}	4.8×10^{7}
Si_3N_4, HfO_2	0.48	68	3.2×10^{-13}	1.8×10^{-5}	5.58×10^{7}

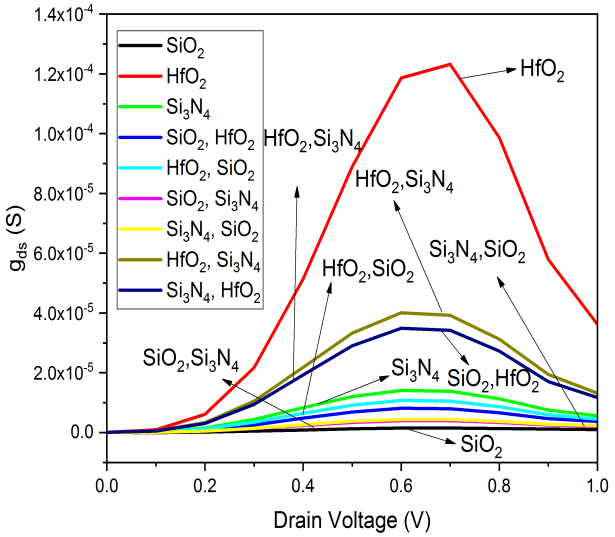


Fig. 8: Variation of Drain conductance with Gate voltage for different dielectric materials

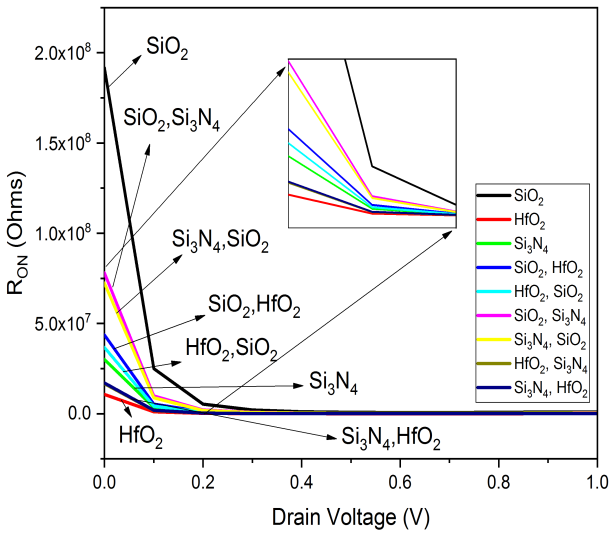


Fig. 9: Variation of On Resistance with Gate voltage for different dielectric materials

rather moderate tunneling rate. SiO_2 is a lower-k dielectric material and produces a weaker electric field at the tunneling junction compared to high-k materials. The weaker field reduces the tunneling probability, hence lower recombination rates. However, the recombination region is more localized, suggesting stable tunneling characteristics at particular zones of the device. Figure 10(b) for HfO_2 has a significantly larger tunneling recombination rate. The high value of dielectric constant of HfO_2 increases the gate control and gives rise to a stronger electric field intensity at the tunneling junction. The better tunneling of carriers with this stronger field shows a higher tunneling recombination rate. The contour covers a larger area, which suggests that the improved region is more dominantly affected by the increased electric field.

Figure 10(c) Si_3N_4 intermediate recombination rates. Si_3N_4 has a higher dielectric constant than SiO_2 but its strength is not as strong as HfO_2. The recombination contours indicate that the electric field and the tunneling efficiency are slightly enhanced, and hence the balanced tunneling rate can be used in applications that require controlled recombination without excessive leakage. Figure 10(d)-(i) introduces tailored effects on the recombination contours through the combination of dielectrics. For instance, Figure 10(d) for $SiO_2 - HfO_2$ and Figure 10(e) for $HfO_2 - SiO_2$ exhibit excellent recombination due to the synergistic effect of high-k HfO_2 and SiO_2 stability. The electric field distribution is optimized to extend the tunneling region with control over the leakage paths. Figure 10(h) for $HfO_2 - Si_3N_4$ and Figure 10(i) ($Si_3N_4 - HfO_2$) have higher recombination rates than Si_3N_4 alone, exploiting the field-enhancing characteristics of HfO_2 while utilizing Si_3N_4's interface stability.

The change of the recombination rate among the different dielectrics is mainly due to differences in electric field intensity and modulation of tunneling barrier. High-k dielectrics such as HfO_2 provide stronger electric fields, which reduces the energy of the tunneling barrier such that more significant numbers of carriers can tunnel through the junction. In contrast, the low-k materials like SiO_2 and moderate-k materials like Si_3N_4 maintain higher tunneling barriers as the recombination rate is reduced. These results clearly emphasize the role of dielectric engineering in TFET design. High-k dielectrics increase tunneling efficiency, while leakage is increased. Combinations of high-k and low-k materials balance the situation for achieving high tunneling

efficiency and leakage suppression. This approach will be highly adaptable to meeting the requirement for different performance aspects required by the electronic devices operating on very low power and high speed.

Figure 11 The contour plots in it depict the tunneling density distribution and intensity throughout the proposed device, thus the effect of several dielectric materials is observed on BTBT tunneling. These plots clearly indicate areas of significant importance for tunneling to take place and how it depends on material properties. Stronger electric fields in the junction occur with high-k dielectrics such as HfO_2, leading to broader and stronger tunneling regions compared to a low-k dielectric material like SiO_2. Such behavior is desirable for improved on-state current along with energy efficiency.

For low-k dielectrics, such as SiO_2, tunneling regions become more localized. The recombination rates are thus moderate because electric fields are much weaker. Thus, it remains stable and allows for lower leakage currents but with reduced on-state current performance. High-k dielectrics like HfO_2 have substantially larger tunneling regions due to their enhanced electric field strength. This property would enhance carrier transport, which implies higher drive currents, though sometimes it increases leakage under off-states.

The tunneling contours of the intermediate behavior of Si_3N_4 are apparent. They show characteristics which follow a balance of the strengths of both low-k and high-k dielectrics. When hybrid dielectric configurations are used, such as $HfO_2 - SiO_2$ or $SiO_2 - Si_3N_4$, the results in the tunneling regions follow an effect of synergism. Such groups improve the efficiency of tunneling by gaining from the electric field strengths of high-k dielectrics. However, they prevent unwanted features such as ultra-high leakage that often characterizes the use of the material alone.

From the contour maps, one can clearly observe that material properties, electric field distribution, and tunneling probabilities significantly affect the performance of devices. High-k and hybrid dielectric materials enable trench control over the tunneling regions, ensuring higher reliability and efficiency levels in low-power and high-speed applications. The above insights highlight the role that dielectric engineering plays in the development of advanced TFET structures.

The contours in Figure 12 show the electron current density along the proposed device structure for different dielectric material configurations. These contour plots clearly illustrate how the dynamic behavior of material properties affects the conduction of currents, and how dielectric engineering better enables electron transport. High-k dielectrics, like HfO_2, have far larger and much more homogeneously distributed regions of current density than the other alloys do, showing they are better gate controlling materials with better carrier mobility enhancements. This behavior directly contributes to improved on-state performance and a higher drive current.

In contrast, low-k materials such as SiO_2 show more restricted and lower-amplitude current density contours, pointing to lower tunneling efficiency and weaker gate-channel coupling. As this leads to superior leakage control and energy efficiency, the modest current flow is insufficient for demanding high-performance applications. The characteristics of moderate-k dielectrics such as Si_3N_4 are balanced because the current density is at an intermediate level, yielding an acceptable trade-off between energy efficiency and performance.

Optimization of current density distribution is attained in hybrid dielectric configurations like $HfO_2 - SiO_2$ and $Si_3N_4 - HfO_2$ through the exploitation of individual material properties. For example, the enhanced tunneling enhancement from HfO_2 combined with the stable interface of Si_3N_4 yields smooth robust electron transport within the device. These hybrid structures improve current density and reduce unfavorable effects such as leakage and short-channel effects.

These variations in the electron current density through different configurations of dielectrics emphasize a material selection and choice as quite important in a TFET-based design. While maintaining high conductivity for current by fine-tuning dielectric property, combining and hybridizing such materials with specific properties can guarantee reduced power loss during conduction. This therefore positions the resultant proposed TFET architecture very well at next-generation-low-power and ultra-high-speed applicative scenarios to easily meet efficiency, coupled with performances.

In Fig. 13, the distribution of hole current density along the structure of the proposed TFET has been revealed across different dielectric material configurations. The images demonstrate how dielectric materials impact the transport of charge carriers and their overall device performance. HfO_2, for instance, as high-k materials results in more and broader regions of hole current density due to enhanced electric field strength, thereby contributing to better on-state performance along with efficient tunneling. This is especially important for obtaining high drive currents in low-power applications.

On the other hand, low-k dielectrics such as SiO_2 have narrower and less intense current density contours, which indicate weaker gate control and a limited ability to enhance tunneling efficiency. These characteristics suppress leakage currents and contribute to energy efficiency but may restrict the capability of the device to deliver high on-state current. Moderate-k materials, such as Si_3N_4, exhibit a balanced performance with current density contours that reflect the trade-off between the benefits of high and low-k dielectrics, thus suitable for applications requiring moderate performance and power efficiency.

Hybrid dielectric combinations like $HfO_2 - SiO_2$ or $Si_3N_4 - HfO_2$ exhibit synergistic behaviors in the hole current density profiles. Combining the tunneling enhancement with high-k materials as well as the stability and leakage suppression from low or moderate-k materials leads to optimized current flow. Hybrid configurations manage all the trade-offs between performance and leakage, providing reliable operation with efficiency across a broad spectrum of applications.

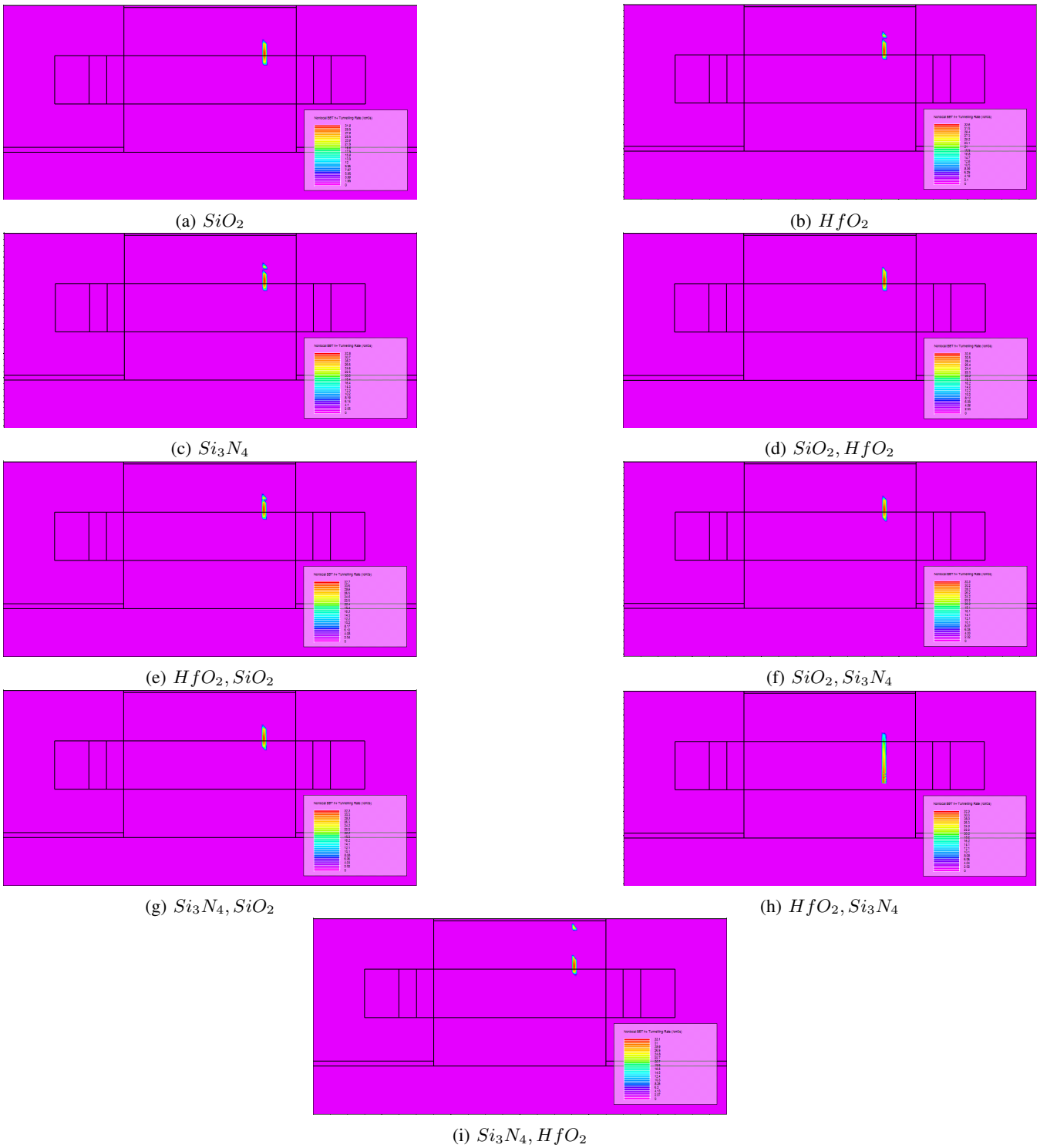
Regarding hole current density distributions, the importance of dielectric material engineering in TFET design is underlined. The device proposed has enhanced carrier transport, reduced leakage, and improved energy efficiency through proper selection and combination of dielectric materials. These findings show the potential of tailored dielectric configurations toward the promise of

(a) SiO_2 (b) HfO_2 (c) Si_3N_4 (d) SiO_2, HfO_2 (e) HfO_2, SiO_2 (f) SiO_2, Si_3N_4 (g) Si_3N_4, SiO_2 (h) HfO_2, Si_3N_4 (i) Si_3N_4, HfO_2

Fig. 10: Contour plots of electron band-to-band tunneling for different dielectric materials, visualizing the tunneling recombination distribution and its dependency on dielectric properties

TABLE III: Performance parameters comparison of Planar TFET and Vertical TFET

Performance Parameter	**Vertical TFET (Proposed)**	**Planar TFET (Typical)**
Threshold Voltage (V_t)	0.37V (HfO_2), -0.67V (SiO_2-Si_3N_4)	~0.5V - 0.7V
Subthreshold Swing (SS) (mV/dec)	49 mV/dec (HfO_2), 88 mV/dec (Si_3N_4-HfO_2)	~60 - 100 mV/dec
On-State Current (I_{on}) (A)	5.8×10^{-5} A (HfO_2)	$\sim 10^{-6}$ - 10^{-5} A
Off-State Current (I_{off}) (A)	3.8×10^{-13} A (HfO_2)	$\sim 10^{-12}$ - 10^{-13} A
I_{on}/I_{off} Ratio	1.5×10^{8} (HfO_2)	$\sim 10^{6}$ - 10^{7}
Gate Control Efficiency	High (Dual-Gate Design)	Moderate
Leakage Current	Low (Optimized Dielectric Layers)	Higher due to Short-Channel Effects
Short-Channel Effects (SCEs)	Suppressed	More Pronounced
Power Consumption	Lower	Higher
Fabrication Complexity	Higher (Vertical Structure, Material Engineering)	Lower (Planar Process)



(a) SiO_2 (b) HfO_2

(c) Si_3N_4 (d) SiO_2, HfO_2

(e) HfO_2, SiO_2 (f) SiO_2, Si_3N_4

(g) Si_3N_4, SiO_2 (h) HfO_2, Si_3N_4

(i) Si_3N_4, HfO_2

Fig. 11: Contour plots of hole band-to-band tunneling for different dielectric materials, illustrating the impact of material selection on hole transport efficiency

(a) SiO_2 (b) HfO_2

(c) Si_3N_4 (d) SiO_2, HfO_2

(e) HfO_2, SiO_2 (f) SiO_2, Si_3N_4

(g) Si_3N_4, SiO_2 (h) HfO_2, Si_3N_4

(i) Si_3N_4, HfO_2

Fig. 12: Electron current density distribution for different dielectric materials, comparing the gate control and carrier transport across the proposed TFET structure.

(a) SiO_2 (b) HfO_2

(c) Si_3N_4 (d) SiO_2, HfO_2

(e) HfO_2, SiO_2 (f) SiO_2, Si_3N_4

(g) Si_3N_4, SiO_2 (h) HfO_2, Si_3N_4

(i) Si_3N_4, HfO_2

Fig. 13: Hole current density distribution for various dielectric materials, showing the effectiveness of high-k dielectrics in enhancing hole carrier mobility

modern electronics for advanced low-power and high-speed applications.

Table II compares key electrical characteristics, which consist of threshold voltage (V_t), subthreshold swing (SS), off-state current (I_{off}), on-state current (I_{on}), and the I_{on}/I_{off} ratio, across the proposed TFET with different dielectric materials and their combinations. The electrical behavior of the designed vertical TFET depends considerably on the dielectric material configuration, as evident from major parameters such as threshold voltage, subthreshold swing (SS), off-state current, and the on-state current. For intrinsic SiO_2, the V_t is 0.75V, showing its poor gate control as a result of low dielectric constant, whereas HfO_2 presents a much smaller V_t of 0.37V as a consequence of high electric field enhancement. Hybrid stacks such as SiO_2-Si_3N_4 display negative threshold voltages of about -0.67V, representing highly efficient tunneling at small gate biases. The subthreshold swing also mirrors the same trend, with HfO_2 achieving an impressive 49 mV/decade, very close to the theoretical limit, over SiO_2's 104 mV/decade, showing better switching behavior in high-k dielectrics.

The values here take different numerical values for each material while reflecting the dependency of dielectric properties on the performance of the device. Table III compares the performance parameters of Vertical TFET and Planar TFET.

A. Threshold Voltage

The threshold voltage changes dramatically depending on the material, from 0.75 V for SiO_2 to -0.67 V for hybrids such as $SiO_2 - Si_3N_4$. Pure SiO_2 will have the highest V_t due to its low dielectric constant, leading to weaker gate control and requiring a greater voltage to begin tunneling. In contrast, the threshold voltage of $HfO_2 - Si_3N_4$ is negative, -0.67 V, meaning the electric field at the tunneling junction is strong due to the large dielectric constant of HfO_2 and a moderate dielectric constant for Si_3N_4. This strong field lowers the energy barrier, enabling tunneling at lower voltages.

B. Subthreshold Slope

The SS values are significantly different, and the lowest SS value of 49 mV/dec is associated with HfO_2, reflecting the best gate-channel coupling of HfO_2. The lower SS means a sharper transition between the off and on states, with a potential for high effectiveness in switching operation. SiO_2 has the largest SS value of 104 mV/dec because of its low dielectric constant that cannot sufficiently suppress the subthreshold leakage. Multi-dielectric configurations such as $HfO_2 - Si_3N_4$ combine the benefits of high-k materials and interface quality improvements to achieve intermediate SS values balancing performance and stability. Table IV shows the summary of electrical characteristics.

C. Off-State Current (I_{off})

The off-state current differs by less than an order of magnitude among materials, typically in the 10^{-13} A range. SiO_2 has the minimum I_{off} of 5.7×10^{-13} A, indicating robust insulating characteristics that minimize leakage in the off-state. HfO_2 shows slightly higher I_{off}, at 3.8×10^{-13} A, because of its dielectric constant, although this dielectric constant improves on-state performance, it can also enhance off-state tunneling probabilities. Multi-dielectric configurations, such as HfO_2-Si_3N_4, have moderate I_{off} values, trading off leakage with performance.

D. On-State Current (I_{on})

The on-state current varies widely, from 8.9×10^{-7} A for SiO2, to 5.8×10^{-5} A for HfO_2, indicating that the high dielectric constant of high-k materials has an important effect on efficient tunneling and carrier transport. The largest value for Ion is demonstrated by HfO_2 as its high dielectric constant reduces the tunneling barrier, allowing the highest number of carriers to pass in the on-state. Other good combinations include $Si_3N_4 - HfO_2$ with a leakage current of 1.8×10^{-5} A, combining HfO_2's tunneling enhancement and Si_3N_4's interface stability.

E. I_{on}/I_{off} Ratio

This ratio of Ion/Ioff varies from 1.5×10^6 for SiO_2 to 1.5×10^8 for HfO_2. The ratio expresses the device's capability of distinguishing between on and off states. Due to better on-current performance and moderate leakage suppression, HfO_2 exhibits the highest ratio. Lower I_{on} and minimal leakage for SiO_2 reduce the ratio. Combinations like Si_3N_4-HfO_2 have an excellent $I_{on} - I_{off}$ ratio at 5.58×10^7, with better performance-leakage balance.

Table I highlights the role of properties of dielectric materials, dielectric constant, quality of the interfaces, and compatibility. The high-k materials like HfO_2 clearly show performance metrics such as I_{on} and an I_{on}/I_{off} ratio that would be appropriate for the development of high-speed, low-power devices. Low-k materials such as SiO_2 with superior leakage suppression have an advantage in ultra-low-power applications. The hybrid configurations combine the strengths of different dielectrics, optimize the electric field distribution, and ensure the reliability of the device under various operating conditions. The dielectric materials applied in the suggested vertical TFET have unique effects on device performance, especially regarding energy band alignment and tunneling properties. Silicon dioxide (SiO_2), a low-k dielectric, has little band alignment shift because of its weaker electric field effect, leading to a high tunneling barrier that restricts carrier injection efficiency. By way of contrast, hafnium oxide, which has a high dielectric constant, creates a significant band alignment shift that strongly lowers the tunneling barrier, allowing for more effective carrier transport.

Comparison of alternative dielectric materials in the offered vertical TFET demonstrates notable variations in performance. HfO_2 dielectrics show minimum threshold voltage with increased device switch capability, while SiO_2 based setups achieve higher threshold voltage, demanding larger energy for their activation. The subthreshold swing is also heavily enhanced using HfO_2, with its 49 mV/dec, compared to the high SiO_2 104 mV/dec value, signifying superior gate control and efficient switch action. The on-state current (I_{on}) is highly variable across the dielectric materials, with HfO_2 showing the highest I_{on} of 5.8×10^{-5} A

TABLE IV: Summary of Electrical Characteristics from Simulation Results

Dielectric Material	Tunneling Region Strength	Carrier Mobility	Leakage Suppression	Electric Field Distribution
SiO_2	Weak	Moderate	Excellent	Localized
HfO_2	Strong	High	Moderate	Extended
Si_3N_4	Moderate	Balanced	Moderate	Even Distribution
$HfO_2 - Si_3N_4$	Strong	High	Good	Extended, Balanced
$SiO_2 - Si_3N_4$	Weak	Moderate	High	Localized

and thus being a good contender for high-speed, low-power applications. SiO_2, on the other hand, has a lower I_{on} because of poor tunneling efficiency. Although high-k dielectrics enhance on-current, they also increase off-state current (I_{off}) marginally, with HfO_2 showing 3.8×10^{-13} A, while SiO_2 provides better leakage suppression with 5.7×10^{-13} A.

IV. Conclusion

In conclusion, the present vertical TFET structure has shown full advancement over conventional MOSFETs and traditional TFETs in addressing the deficiencies. The method utilized innovative dual-gate architecture, heterostructure materials, optimized dielectric configurations, with superior tunneling efficiency, low threshold voltage, and enhanced drive current performance achieved by the device. The low subthreshold swing, minimal leakage currents, and robust I_{on}/I_{off} ratio of the device validated its simulation results as being suitable for low-power and high-speed applications. TFETs show good reliability performance with minimized short-channel effects through careful selection of materials and design parameters. This contribution emphasizes how TFETs can fill the gap between the two major challenges presently: energy efficiency and scaling.

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