Differential Difference Gain Amplifier (DDGA) and Its Applications

Jetsdaporn Satansup, Tattaya Pukkalanun* and Worapong Tangsrirat, *Member, IAENG*

***Abstract*—This article introduces a CMOS circuit realization of the fully balanced differential difference gain amplifier (DDGA). The proposed DDGA is realized using four floating current sources operating under dual supply voltages of approximately ±0.9 V. The proposed circuit can function as a differential difference gain amplifier with electronically adjustable gain both in voltage and current-modes. The application designs of the DDGA to implement a single-input three-output universal biquad filter and voltage-mode quadrature oscillator circuit are also suggested. PSPICE simulation results for the proposed DDGA and its applications are provided using 0.18-μm CMOS technology from TSMC.**

***Index Terms*—Differential Difference Gain Amplifier (DDGA), universal filter, quadrature oscillator, transconductance amplifier, voltage-mode circuits**

I. Introduction

SINCE the introduction of the current differencing amplifier, or Norton amplifier, in 1970, it has been known as the first active building block with the current difference property [1]. Subsequently, the operational transresistance amplifier (OTRA) [2], differential current conveyor (DCCII) [3], current differencing buffered amplifier (CDBA) [4]–[5], and current differencing transconductance amplifier (CDTA) [6]–[7] all received significant attention in the scholarly literature. The input stage of these active elements comprises the so-called current-difference circuit, which is equipped with two low-impedance terminals. Additionally, the DCCII incorporates an extra voltage input terminal. In 2008, a collection of novel active building blocks was reviewed and introduced as the counterparts of current differencing-based active building blocks, as previously described [8]. The current-difference circuit in these devices is replaced by a voltage-difference circuit, which is implemented by employing an operational transconductance amplifier (OTA) [9]. By employing this approach, the CDBA is converted into a conversion into a voltage-difference buffered amplifier (VDBA) [8], [10]. This transformation subsequently gives rise to a voltage-difference input buffered amplifier (VD-DIBA) [11], which, along with the voltage-difference transconductance amplifier (VDTA) and voltage-difference inverting buffered amplifier (VDIBA), has been utilized in several analog signal processing applications [12]–[18].

Since its first definition in 2013 [19], a voltage differencing gain amplifier (VDGA), a recently introduced active element, has gained significant popularity in recent years [20]–[25]. In continuation of the previous work, this paper introduces a novel voltage-difference-based active device, called differential difference gain amplifier (DDGA), which may serve as a versatile active building block for analog signal processing applications and solutions. The proposed DDGA consists of four floating current sources (FCSs) [26], each performing as an independent transconductance amplifier to provide electronically tunable circuit transfer gains. This work also introduces a new single-input three-output (SITO) universal filter with all grounded components based on a single presented DDGA. Furthermore, a single DDGA-based voltage-mode quadrature oscillator is demonstrated. The rest of this paper is organized as follows: Section 2 outlines the concept and description of the proposed fully balanced DDGA circuit. Section 3 discusses the functional verification and simulation results for the realized DDGA. Thereafter, application examples of the proposed DDGA, including the SITO universal biquad filter and quadrature oscillator, are introduced in Section 4. Finally, Section 5 serves as the conclusion of this work.

II. Concept and Description of The Proposed DDGA

Conceptually, the DDGA is a special type of fully balanced difference amplifier with electronically tunable gain capability, as symbolically depicted in Fig. 1. In this device, the input voltage terminals p1, p2, n1, and n2 are characterized by high impedance, while the terminals z+, z-, and o exhibit high-impedance output current terminals. Furthermore, the w terminal serves as the output voltage terminal with low impedance. The voltage difference between the differential input voltages supplied across the p_1 and n_1 terminals (v_{p1}-v_{n1}) and the p_2 and n_2 terminals (v_{p2}-v_{n2}) is transformed into the output currents at the terminals z+ and z- through the transconductance gains. The voltage across the terminal z+ (v_{z+}) is then amplified to the output voltage at the w terminal (v_w) and also converted to the output current at the o terminal (i_o). As a result, the ideal DDGA characteristic can be defined by the following hybrid matrix:

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$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ i_o \\ v_w \end{bmatrix} = \begin{bmatrix} g_{mA} & -g_{mA} & -g_{mB} & g_{mB} & 0 \\ -g_{mA} & g_{mA} & g_{mB} & -g_{mB} & 0 \\ 0 & 0 & 0 & 0 & g_{mC} \\ 0 & 0 & 0 & 0 & \beta \end{bmatrix} \begin{bmatrix} v_{p1} \\ v_{n1} \\ v_{p2} \\ v_{n2} \\ v_{z+} \end{bmatrix}, \quad (1)$$

where g_{mA}, g_{mB}, and g_{mC} denote the small-signal transconductance gain and β represents and voltage gains of the DDGA. Due to the presence of two differential high-input impedance terminals, the DDGA is well-suited for the processing of fully differential input signals. Furthermore, it possesses the benefit of including electronically adjustable gains, a crucial feature in numerous analog signal processing applications.

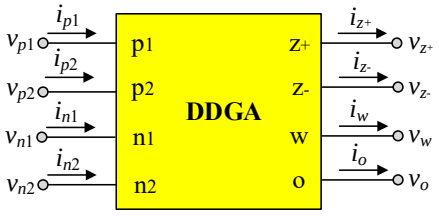


Fig. 1. Schematic symbol of the DDGA element.

As explained in (1), the behavior model of the proposed DDGA can be symbolized by a simplified block diagram in Fig. 2(a), while Fig. 2(b) depicts the CMOS circuit implementation derived from the model delineated in Fig. 2(a). The circuit architecture of this CMOS DDGA is designed with four FCSs, formed by transistors M_{1k}–M_{9k} (where k represents A, B, C, and D) [26]. Each of these cells exhibits the independently tunable transconductance gain g_{mk}, as determined by [19]:

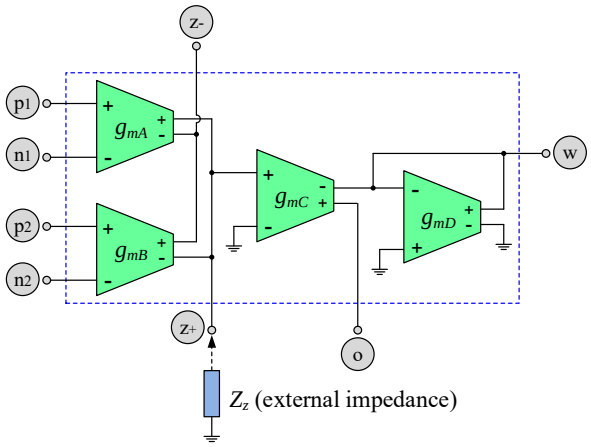
$$g_{mk} = \left(\frac{g_{1k}g_{2k}}{g_{1k}+g_{2k}}\right) + \left(\frac{g_{3k}g_{4k}}{g_{3k}+g_{4k}}\right), \quad (2)$$

where

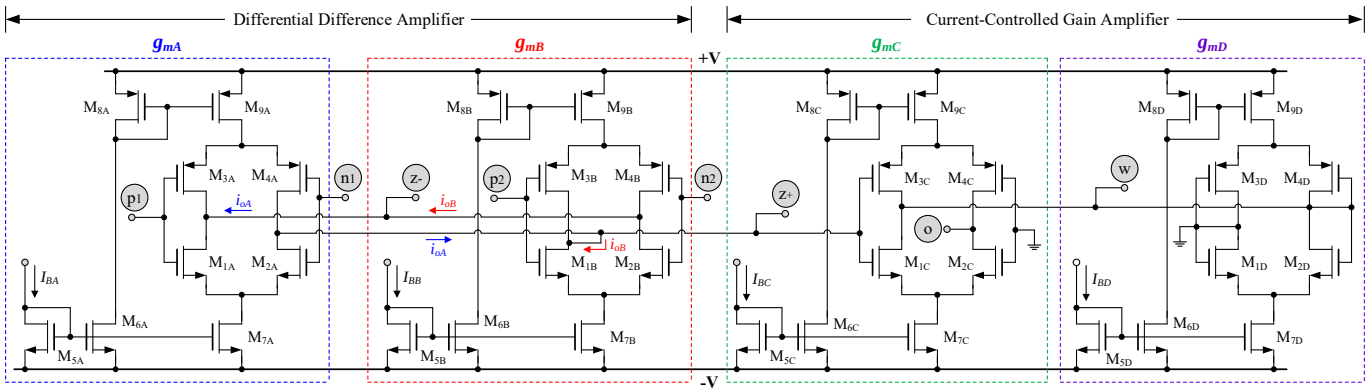
$$g_{ik} = \sqrt{\left(\frac{\mu C_{ox} W_i}{L_i}\right) I_{BK}}, \quad (3)$$

for i = 1, 2, 3, and 4. In above expressions, I_{Bk} is the external DC bias current, μ is the free carrier mobility in the channel, Cox is the gate-oxide capacitance per unit area, and W_i and L_i are the channel width and length of the transistor M_{ik}, respectively. Based on (2) and (3), it is evident that the g_{mk}-value can be tuned electronically by simply adjusting the related bias current I_{BK}.

According to Fig. 2(b), the FCSs M_{1A}–M_{4A} and M_{1B}–M_{4B} both perform the differential-input voltage to current converter, i.e., $i_{oA} = g_{mA}(v_{p1}-v_{n1})$ and $i_{oB} = g_{mB}(v_{p2}-v_{n2})$. As a result, the currents at z+ and z- terminals are equal to the difference between the currents i_{oA} and i_{oB}, (or $i_{z+} = i_{oA} - i_{oB}$ and $i_{z-} = i_{oB} - i_{oA}$), respectively. The FCS M_{1C}-M_{4C} will transfer the voltage across terminal z+ (v_{z+}) into the current at the o terminal (or $i_o = g_{mC}v_{z+}$).



(a)



(b)

Fig. 2. Concept and description of the proposed DDGA element:
(a) behavior model (b) CMOS circuit realization

In addition, a pair of FCSs M_{1C}–M_{4C} and M_{1D}–M_{4D} functions as a current-tunable voltage amplifying action between z and w terminals ($v_w = \beta v_z$). Thus, the voltage transfer gain β of the DDGA may be mathematically expressed as:

$$\beta = \frac{g_{mC}}{g_{mD}}, \tag{4}$$

which can be set electronically by means of I_{BC} and I_{BD}. Given equal transconductance, i.e., $g_{mnC} = g_{1C} = g_{2C}$, $g_{mpC} = g_{3C} = g_{4C}$, $g_{mnD} = g_{1D} = g_{2D}$, and $g_{mnD} = g_{3D} = g_{4D}$, we can determine the maximum value for the gain β of the proposed DDGA as follows:

$$\beta_{\max} = \frac{\left(g_{mnC} + g_{mpC}\right)_{\max}}{\left(g_{mnD} + g_{mpD}\right)_{\min}} . \tag{5}$$

This expression shows that the highest possible value of β can be achieved by setting the values of g_{mnC} and g_{mpC} to their maximums, while keeping the values of g_{mnD} and g_{mpD} at minimums.

III. Functional Verification and Simulation

The performance of the proposed DDGA shown in Fig. 2(b) has been examined using PSPICE simulation. A simulation of the CMOS DDGA circuit was conducted utilizing 0.18-µm CMOS real process parameters obtained from TSMC (Taiwan Semiconductor Manufacturing Company, Ltd.). The bias voltages used were set to be ±V = ±0.9 V. The aspect ratios of the CMOS transistors used in simulation are listed in Table I.

TABLE I
Transistors Aspect Ratios of the DDGA shown in Fig. 2(b).

Transistors	Aspect Ratios, W/L (µM/µM)
M_{1k}, M_{2k}	24/0.18
M_{3k}, M_{4k}	30/0.18
M_{5k}, M_{6k}, M_{7k}	5/0.18
M_{8k}, M_{9k}	6/0.18

Fig. 3 illustrates the output currents from z+ and z- terminals of the DDGA as a function of the differential input voltage ($v_{p1} - v_{n1}$) applied to p1 and n1 terminals, when the voltage ($v_{p2} - v_{n2}$) was kept constant at 25 mV. The set of curves represents different values of the transconductance g_{mA}, considering a constant g_{mB} of 1 mA (I_{BB} = 80 µA). In contrast, the simulated output currents i_{z+} and i_{z-} against the differential input voltage ($v_{p2} - v_{n2}$) at a value of ($v_{p1} - v_{n1}$) = 25 mV are shown in Fig. 4. Fig.5 shows the frequency responses of the transfer voltage between v_z and v_w with β tuning. The values of β = 1.30, 1.53, 1.70, and 1.90 were obtained by adjusting the g_{mC} value to 1.30 mA/V, 1.53 mA/V, 1.70 mA/V, and 1.90 mA/V, respectively, while still keeping the g_{mD} value constant at 1 mA/V. The AC analysis results show that the maximum operating frequency for this stage is approximately more than 100 MHz. At I_{Bk} = 80 µA, the total standby power consumption was around 1.75 mW.

The frequency responses of the input resistances at terminals p1, p2, n1, and n2 (R_{p1}, R_{p2}, R_{n1}, and R_{n2}) for the realized DDGA are shown in Fig. 6. The output resistances at terminals z+, z-, o, and w (R_{z+}, R_{z-}, R_o, and R_w) with respect to frequency are also given in Figs.7 and 8, respectively. The terminal resistances at low frequencies, as determined by the small-signal PSPICE simulation, were found to be $R_{z+} = R_{z-}$ = 24 kΩ, R_o = 48 kΩ, and R_w = 1.02 kΩ. It is noteworthy that all circuit simulation results exhibit agreement with theoretical expectations.

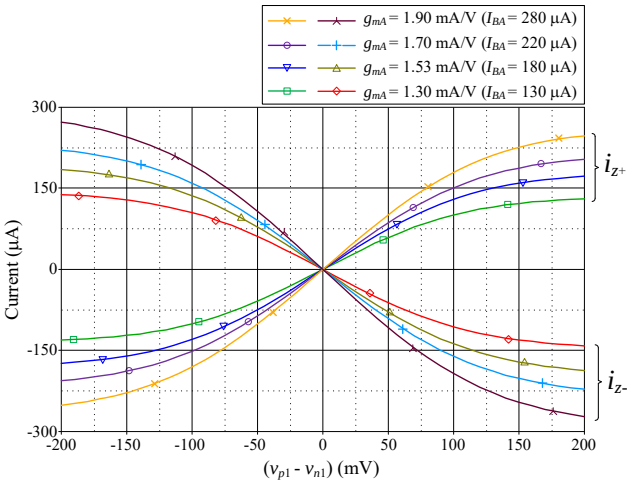


Fig. 3. Output currents i_{z+} and i_{z-} with respect to the differential input voltage ($v_{p1} - v_{n1}$).

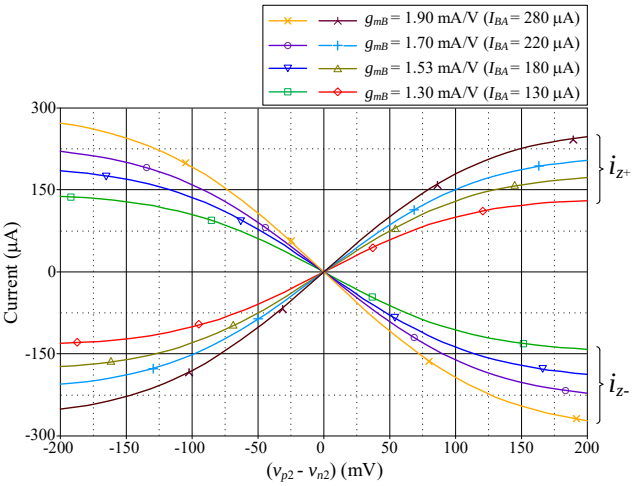


Fig. 4. Output currents i_{z+} and i_{z-} with respect to the differential input voltage ($v_{p2} - v_{n2}$).

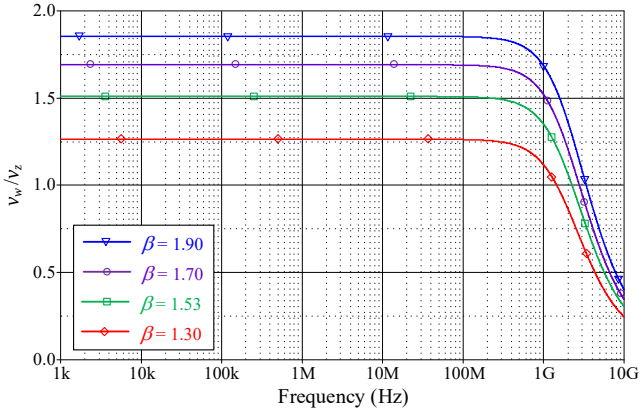


Fig. 5. Frequency responses of voltage transfer gain (v_w/v_z).

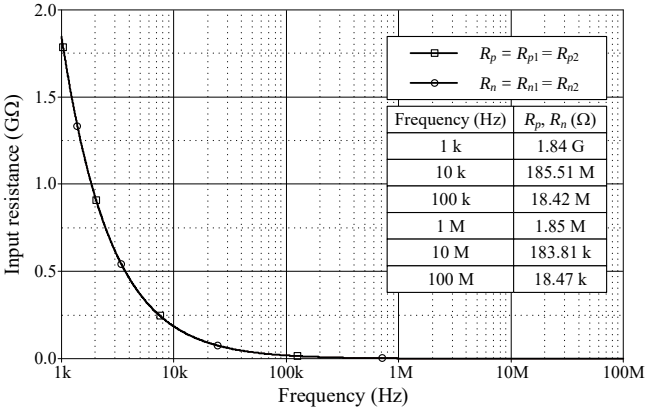


Fig. 6. Frequency responses of the input resistances R_{p1}, R_{p2}, R_{n1}, and R_{n2}.

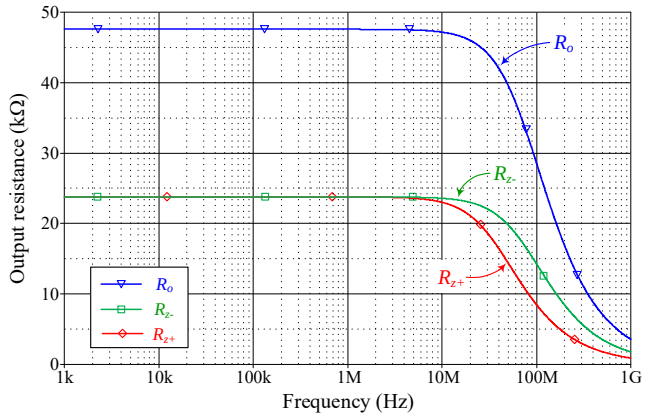


Fig. 7. Frequency responses of the output resistances R_{z+}, R_{z-}, and R_o.

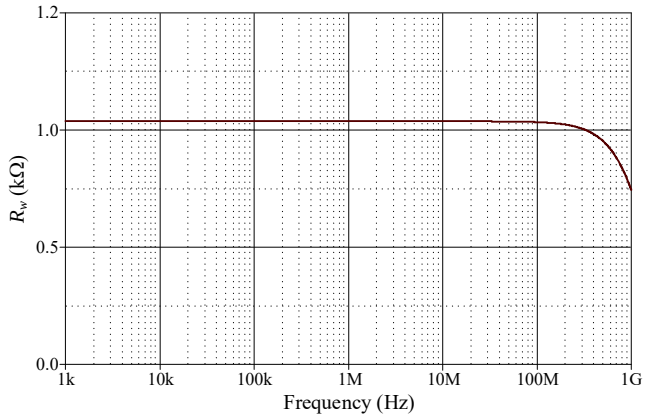


Fig. 8. Frequency response of the output resistance R_w.

IV. Applications of the Proposed DDGA

This section introduces the use of the proposed DDGA in realizing a single-input three-output multifunction biquad filter and voltage-mode quadrature oscillator circuit as application examples. In both circuit designs, one should recognize the advantage of using only a single DDGA as an active element.

A. Single DDGA-based multifunction biquad filter realization

Fig. 9 shows the DDGA-based multifunction biquad filter realization. It contains a single DDGA, a grounded resistor, and two grounded capacitors, making it suitable for integration. The circuit analysis provides the lowpass (LP), bandpass (BP), and highpass (HP) voltage responses at different nodes, represented by the following transfer functions:

$$T_{LP}(s) = \frac{V_{LP}(s)}{V_{in}(s)} = \frac{A_{LP}\left(\frac{g_{mA}g_{mC}}{C_1C_2}\right)}{D(s)} \quad , \tag{6}$$

$$T_{BP}(s) = \frac{V_{BP}(s)}{V_{in}(s)} = \frac{A_{BP}\left(\frac{g_{mB}g_{mC}}{g_{mD}C_1}\right)s}{D(s)} \quad , \tag{7}$$

and

$$T_{HP}(s) = \frac{V_{HP}(s)}{V_{in}(s)} = \frac{A_{HP}s^2}{D(s)} \quad , \tag{8}$$

where

$$D(s) = s^2 + \left(\frac{g_{mB}g_{mC}}{g_{mD}C_1}\right)s + \left(\frac{g_{mA}g_{mC}}{C_1C_2}\right) \quad , \tag{9}$$

$$A_{LP} = 1 \quad , \quad A_{BP} = \frac{g_{mA}g_{mD}}{g_{mB}g_{mC}} \quad , \text{and} \quad A_{HP} = -g_{mA}R_1 \tag{10}$$

It can be seen that the LP, BP, and HP filter functions are obtained from the output nodes v_{LP}, v_{BP}, and v_{HP}, respectively. In consequence, the suggested filter can be considered a configuration with single input and three output terminals. Furthermore, the circuit does not require any component-matching conditions for realizing transfer functions.

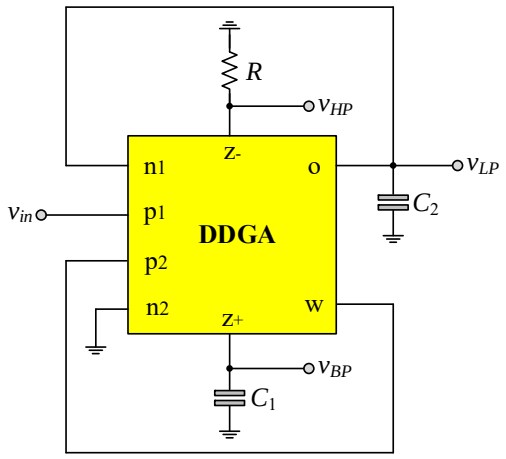


Fig. 9. Single DDGA-based universal biquad filter.

Equations (6)-(10) characterize the filter responses with the natural angular frequency (ω_n) and the quality factor (Q) as follows:

$$\omega_n = 2\pi f_n = \sqrt{\frac{g_{mA}g_{mC}}{C_1C_2}} \quad , \tag{11}$$

and

$$Q = \left(\frac{g_{mD}}{g_{mB}}\right)\sqrt{\frac{g_{mA}C_1}{g_{mC}C_2}} \quad . \tag{12}$$

For a practically simple design, if we set $g_m = g_{mA} = g_{mC}$ and $C = C_1 = C_2$, equations (11) and (12) can then be modified as:

$$\omega_n = \frac{g_m}{C} \quad , \tag{13}$$

and $$Q = \frac{g_{mD}}{g_{mB}} \quad . \tag{14}$$

In (13) and (14), the important parameters ω_n and Q are independently adjustable. Equation (14) also demonstrates that a moderate value of the g_{mD}/g_{mB} ratio can effectively achieve the high-Q filter design.

To validate the theory, the single DDGA-based universal biquad filter in Fig. 9 has been simulated with PSPICE program. The designed parameters are g_{mk} = 1 mA/V, R_1 = 1 kΩ, and C_1 = C_2 = 100 pF, to achieve the filter responses with f_n = 1.59 MHz and Q = 1 theoretically. Fig. 10 displays the simulated LP, BP, and HP frequency characteristics of the filter. The simulated f_n equals 1.52 MHz, which closely approximates the theoretical value. The time-domain responses of the circuit are also given in Fig. 11 for a sinusoidal input signal with a frequency of 1.59 MHz and a peak amplitude of 50 mV.

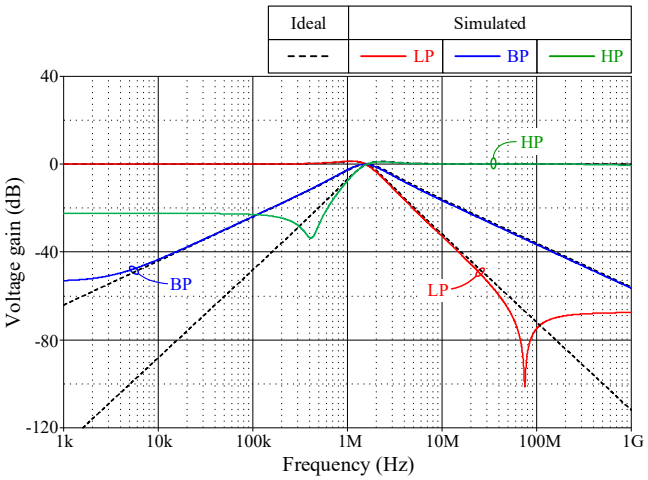


Fig. 10. Simulated time-domain responses of the universal filter in Fig. 9.

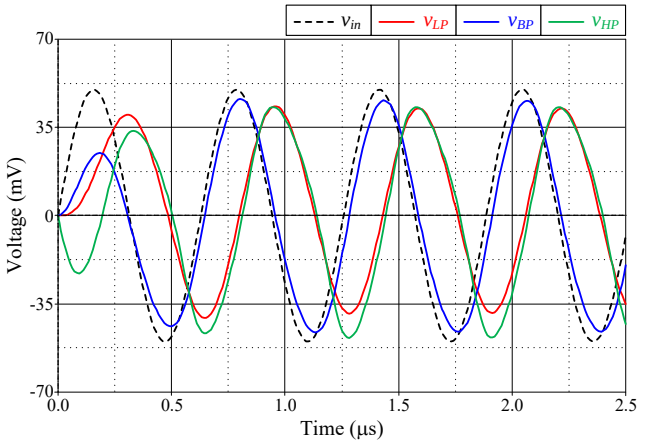


Fig. 11. Ideal and simulated frequency responses of the universal filter in Fig. 9.

B. *Single DDGA-based quadrature oscillator realization*

The quadrature oscillator (QO) circuit based on using the proposed DDGA as an active element is illustrated in Fig. 12. The circuit comprises a single DDGA, two capacitors, and a voltage buffer, producing two quadrature output voltages v_{o1} and v_{o2}. It should be noted that the voltage buffer is implemented by a simple MOS source follower. In Fig. 12, the characteristic equation of the QO can be expressed as:

$$s^2 + \left[\frac{g_{mA} - (g_{mA} + g_{mB})V_C}{C_1} + \frac{g_{mC}}{C_2}\right]s + \left(\frac{g_{mB}g_{mC}}{C_1C_2}\right) = 0 \quad . \tag{15}$$

Therefore, the condition of oscillation (CO) is given by:

$$V_C = \frac{g_{mA}C_2 + g_{mC}C_1}{(g_{mA} + g_{mB})C_2} \quad , \tag{16}$$

and the frequency of oscillation is obtained as:

$$\omega_{osc} = 2\pi f_{osc} = \sqrt{\frac{g_{mB}g_{mC}}{C_1C_2}} \quad . \tag{17}$$

Equations (16) and (17) suggest that the control voltage V_C can independently tune the CO, whereas the transconductances g_{mB} and/or g_{mC} can also electronically control the ω_{osc}. As a consequence, the advantage of the suggested QO circuit in Fig. 12 is that both the parameters CO and ω_{osc} can be tuned orthogonally using a simple electronic method.

The configuration in Fig. 12 produces the voltage transfer function from v_{o1} to v_{o2} as follows:

$$\frac{v_{o2}(j\omega)}{v_{o1}(j\omega)} = \left(\frac{g_{mD}}{\omega C_2}\right)e^{-j90^\circ} \quad . \tag{18}$$

In (18), the phase difference between v_{o1} and v_{o2} is precisely 90°. Hence, the output voltages v_{o1} and v_{o2} are to be expressed as quadrature.

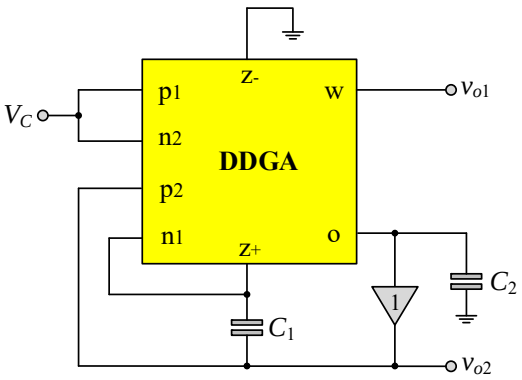


Fig. 12. Single DDGA-based quadrature oscillator.

As a design example, the QO circuit given in Fig. 12 has been simulated with the following component values: g_{mk} = 1 mA/V, C_1 = C_2 = 100 pF, and V_C = 1 V. The designed oscillation frequency was obtained as: f_{osc} = 1.59 MHz. Fig. 13 shows the steady-stage waveforms of the quadrature voltages v_{o1} and v_{o2}. From the results, the simulated f_{osc} was determined to be 1.36 MHz. The simulated phase difference between v_{o1} and v_{o2} was found to be 91.56°, indicating the absolute phase error of less than 1.80%. Furthermore, the quadrature relationship between the generated waveforms has been confirmed using Lissajous plot depicted in Fig. 14.

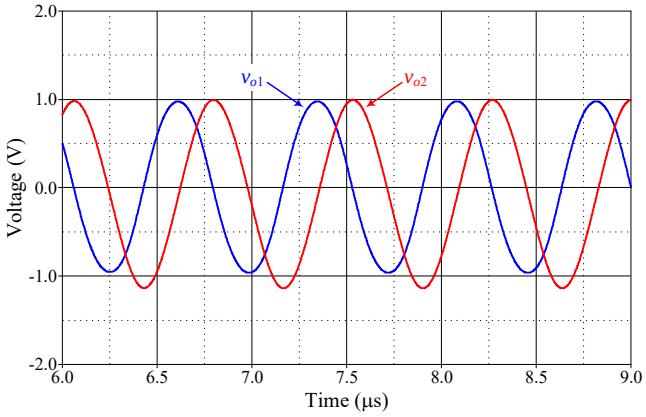


Fig. 13. Steady-state responses of v_{o1} and v_{o2} for the QO in Fig. 12.

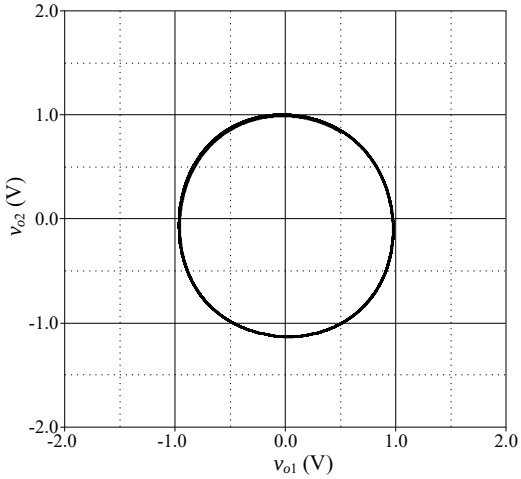


Fig. 14. Lissajous plot of the QO in Fig. 12.

V. Conclusions

This paper proposes a CMOS realization for the fully balanced differential difference gain amplifier (DDGA). The realization is based on using only floating current sources for both input and output stages. The proposed DDGA provides fully balanced differential input signals, as well as electronically variable gain amplifiers. It is also appropriate for mixed-mode applications where fully differential signal processing is required. Applications to the proposed DDGA include a SITO universal filter and a voltage-mode quadrature oscillator, both of which use a single DDGA. All circuits are examined with PSPICE simulation using TSMC 0.18-µm CMOS process parameters and symmetrical bias voltages of ±0.9 V to validate the theoretical predictions.

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