# Deadbeat Model Predictive Control with Virtual Voltage-Vectors to Achieve Constant Common-Mode Voltage for Three-Level T-type Converters Considering Dead-Time Effects

Jingmei Guo, Chao Sheng, Youzhi Zeng, Qinglan Tang, Qing Su

Abstract—Three-level converters have received great attention in common-mode-voltage (CMV) suppression due to their potential to achieve zero- or constant CMV. To achieve constant CMV under the influence of dead time (DT) effects, the use of model predictive control (MPC) provides the possibility. However, the fewer candidate vectors lead to a deterioration in power quality and there may still be some CMV spikes present. To achieve constant CMV as well as maintain high-quality current output, a deadbeat model predictive control with virtual voltage-vector (DB-MPCVV2) is proposed. First, based on the constant CMV analysis of threelevel T-type converter (3LT2C) considering DT, virtual voltagevectors (VV2s) are established. Second, to alleviate the computational burden, deadbeat (DB) control is used. Finally, a specific control method based on the 7th current sector has been proposed to avoid the potential CMV spikes caused by current polarity misjudgment. Simulation and experimental results show that the proposed DB-MPCVV<sup>2</sup> method can effectively achieve constant CMV while maintaining high power-quality current output.

Index Terms — common-mode voltage (CMV), dead-time (DT), virtual voltage-vector ( $VV^2$ ), power quality.

### I. INTRODUCTION

VOLTAGE source inverter plays an important role in a wide range of grid-connected photovoltaic (PV), active power filter and motor drive systems [1-5]. However, its inherent common-mode voltage (CMV) problem limits its further development. The large variation in CMV will not only lead to leakage current, motor insulation failure and other problems [6-8], but also produce electromagnetic

Manuscript received Nov 28, 2024; revised May 20, 2025.

This work was supported by Guangdong Provincial Key Laboratory of New Technology for Smart Grid, China Southern Power Grid Technology Co., Ltd Guangzhou, Guangdong 5100, China. NO: GDKJXM20240547.

Jingmei Guo is a senior engineer at Guangdong Provincial Key Laboratory of New Technology for Smart Grid, China Southern Power Grid Technology Co., Ltd. Guangzhou, Guangdong 5100, China (Email: gjm\_gddky@163.com).

Chao Sheng is a professor level senior engineer at Guangdong Provincial Key Laboratory of New Technology for Smart Grid, China Southern Power Grid Technology Co., Ltd. Guangzhou, Guangdong, 5100, China (Email: chaosheng@gd.csg.cn).

Youzhi Zeng is an engineer at Guangdong Provincial Key Laboratory of New Technology for Smart Grid, China Southern Power Grid Technology Co., Ltd. Guangzhou, Guangdong 5100, China (Email: youzhizeng@163.com).

Qinglan Tang is an engineer at Guangdong Provincial Key Laboratory of New Technology for Smart Grid, China Southern Power Grid Technology Co., Ltd. Guangzhou, Guangdong 5100, China (Email:1413573404@ qq.com).

Qing Su is an engineer at Guangdong Provincial Key Laboratory of New Technology for Smart Grid, China Southern Power Grid Technology Co., Ltd. Guangzhou, Guangdong 5100, China (Email: suqin@gd.csg.cn). interference (EMI) noise which is detrimental to sensitive electronic components in the whole system, resulting in the collapse of system. Currently, there are some ways to suppress CMV [9, 10]. 1) Using active or passive filters. 2) Inverter topology improvement. 3) Control method improvement [11-13].

The use of active or passive filters allowed the inverter to suppress CMVs while considering other performance [14]. However, this method would make the cost and volume of the entire inverter system unsatisfactory. Topology improvement may alleviate this problem to some extent. Topology improvement requires the addition of additional devices to the conventional inverter topology. For example, additional switches were added to the three-phase two-level inverter to form the H7, H8 and H10 topology [15-18]. This type of topology all share a common feature: They limit the overall CMV amplitude by operating additional switches during the zero-voltage-vectors (ZVVs). Further, on the basis of the H8 topology, diodes or capacitors were added to obtain a better CMV suppression effect [19, 20]. But the topology improvements mentioned above could reduce CMV by up to 66% at the cost of power quality and modulation index. To optimize the overall performance of inverter, some improved topologies which consider both the boost capacity and the CMV suppression were developed. For instance, in [21], a modified impedance source inverter was proposed. Its CMV is suppressed to one-sixth of the DClink voltage ( $V_{dc}$ ) and the output voltage gain is enhanced. However, the choice of inductors and capacitors in this topology increases the complexity of the system design and the system loss inevitably increases. In [22], T. T. Tran et al. proposed a novel three-phase constant CMV inverter (CCMVI) based on the switched-capacitor voltage multiplier. Although the  $V_{dc}$  of CCMVI is stepped up to triple of the input voltage, it is worth noting that the inrush current of the capacitors and high conduction loss are the main drawbacks.

To reduce the number of additional devices and improve the CMV suppression ability, many improved control methods are used in inverters. In [23] and [24], active zero state PWM (AZSPWM) or near state PWM (NSPWM) pulse-width-modulation (PWM) strategies were used, the CMV could be reduced by 66.6%. However, these modulations exclude the ZVVs thus leading to the deterioration of total harmonic distortion (THD). To eliminate this drawback, multilevel inverter topologies can be used. In [25], an improved virtual space vector pulse-width-modulation strategy with three-level neutral point clamped converter (3L-NPC) was proposed, the amplitude

of CMV was suppressed within  $\pm V_{dc}/6$ . To achieve constant CMV, a six medium and one zero vectors (6MV1Z) modulation was presented based on 3L-NPC topology [26]. The reference voltage vector (VV) was composed by using only the medium vectors and the zero vector. Similarly, in [27], an easy-to-implement 6MV1Z modulation based on a novel three-level embedded-switch inverter (ESI) topology was proposed. In addition, discrete space vector modulation (DSVM) was used in 3L-NPC to achieve constant CMVs and high power quality current output [28, 29]. However, these methods do not consider the influence of the dead-time (DT).

To prevent the short circuit through of voltage converters, DT control are usually inserted between the gate signals of two switches in one leg, but the DT may cause unexpected CMV spikes. To address this issue, model predictive control (MPC) technology was improved in [30-34]. In [30], the CMV-generated pattern during the DT between two active voltage vectors was analyzed and the proposed method not only allowed all vector transitions without the peak CMVs but also improved the current THD. However, it is still a large CMV range ( $V_{dc}/4$  to  $3V_{dc}/4$ ). In [31] and [32], all the VV switching combinations that may generate CMV spikes during DT were pre-excluded, the range of CMV was significantly reduced. However, the reduced number of the candidate VVs leads to an increase in the current THD. In [33], a hybrid VV preselection strategy which makes full use of the six nonzero VVs was proposed to reduce current THD and eliminate the effects of current polarity misjudgment during the zero crossing which also may incur CMV spikes.

From the existing literature reviews, it is clear that there is a need to offer superior power quality and achieve constant CMV considering DT effect. Inspired the CMV analysis during DT of three-level T-type converter (3LT<sup>2</sup>C) in [35]. A deadbeat model predictive control with virtual voltagevector (DB-MPCVV<sup>2</sup>) is proposed. The DB-MPCVV<sup>2</sup> has some features: 1) Virtual voltage-vectors (VV<sup>2</sup>s) are established to improve the power quality of the output voltage. 2) The deadbeat (DB) control is used to alleviate the computational burden. 3) The potential CMV spikes are eliminated by adding the 7th current sector. In summary, the main contributions can be concluded as follows:

- 1) Based on the constant CMV analysis of 3LT<sup>2</sup>C in [28] and [35], the VV<sup>2</sup>s considering DT are proposed. Thus, the reduction on the THD of the output current can be achieved.
- 2) According to the DB control, the control strategy in space vector area of each current sector is divided into three cases, which alleviate the computational burden and full range utilization of the modulation index.
- 3) Based on the hybrid VV preselection strategy in [33], the 7th current sector is also considered and the theoretical basis for designing the 7th current sector is also be provided, the results indicating that this technique could eliminate CMV spikes caused by current polarity misjudgment.

The arrangement of this article is as follows: Section II introduces the CMV problem of 3LT<sup>2</sup>C topology considering DT. In Section III, model of the 3LT<sup>2</sup>C is presented, and the corresponding prediction equation is established. In addition, this section describes the design and implementation of the proposed DB-MPCVV<sup>2</sup> method, and a block diagram of the DB-MPCVV2 is presented.

Simulation and experimental results are presented in Sections IV and V, which validate the effectiveness of the proposed method. Finally, Section VI concludes this article.

#### II. ANALYSIS OF CMV FOR 3LT<sup>2</sup>C TOPOLOGY

#### A. Topology of a Three-Level T-type Converter $(3LT^2C)$

The structure of a 3LT<sup>2</sup>C VSI topology is shown in Fig. 1 and this topology consists of twelve insulated-gate-bipolartransistor (IGBT) power switches and two capacitor dividers. IGBT  $T_{x2}$  and  $T_{x3}$  form the horizontal bridge arms,  $T_{x1}$  and  $T_{x4}$  form the vertical bridge arms (x = a, b, c).

The state of each phase can be represented by the vectors "1", "-1" and "0", and the switching states of the four IGBTs in each phase, the output voltage has three voltage levels, as given in Table I.

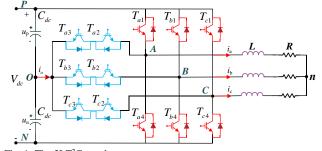


Fig. 1. The 3LT<sup>2</sup>C topology.

TABLE I Switching States of the  $3LT^2C$  Topology

Vector	$T_{x1}$	$T_{x2}$	$T_{x3}$	$T_{x4}$	$V_{ m out}$
1	ON (1)	ON (1)	OFF	OFF	$V_{dc}/2$
			(0)	(0)	
0	OFF (0)	ON (1)	ON (1)	OFF	0
-1	OFF (0)	OFF(0)	ON (1)	(0)	$-V_{dc}/2$
				ON (1)	

Since each phase contains three vector states, the 3LT<sup>2</sup>C topology has a total of 27 VVs: six long vectors, six medium vectors, twelve small vectors, and three zero vectors. The space voltage vector diagram of 3LT<sup>2</sup>C is shown in Fig. 2.

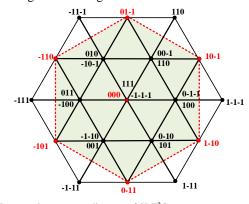


Fig. 2. Space voltage vector diagram of 3LT2C converter.

The CMV of the 3LT<sup>2</sup>C topology could be defined as (1):  

$$V_{CM} = (\frac{V_{AN} + V_{BN} + V_{CN}}{3})$$
(1)

where  $V_{CM}$  is CMV.  $V_{AN}$ ,  $V_{BN}$ , and  $V_{CN}$  are the voltages between points A-N, B-N, and C-N, respectively.

According to the definition of CMV, all CMV values are listed in Table II. Obviously, to reduce the variation range of CMV, it is necessary to limit the use of VVs. It may be observed that in order to obtain a constant CMV, it is a good

TABLE II
Relationship between the VVs and CMV

Voltage vectors	CMV
111	$V_{dc}$
011,101,110	$5V_{dc}/6$
100, 010, 001, -111,1-11,11-1	$2V_{dc}/3$
000, 01-1, -110, -101, 0-11, 1-10, 10-	$V_{dc}/2$
1	
-100,0-10,00-1,1-1-1, -11-1, -1-11	$V_{dc}/3$
0-1-1, -10-1, -1-10	$V_{dc}/6$
-1-1-1	0

choice to use six medium vectors and one zero vector (6MV1Z: 000,01-1,-110,-101,0-11,1-10,10-1) [26].

#### B. CMV Problem Considering Dead-Time.

Semiconductor devices are non-ideal switches, the DT is inevitably needed in practical application to prevent the shoot-through faults. New switching states will be generated during DT and Fig. 3 depicts the new six switching states ( $DT_{(x)}$ , x = 1-6). When the inverter is operating in one of the six switching states, the CMV spikes may occur and this needs to be analyzed in conjunction with the output current of inverter. The sectors and current directions are summarized in Table III.

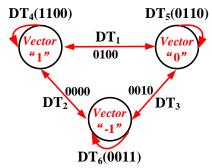


Fig. 3. The new switching states during DT in 3LT<sup>2</sup>C.

#### TABLE III CURRENT SECTOR DIVISION

Sector	Current	Sector	Current
1	$i_a>0, i_b<0, i_c>0$	4	$i_a < 0, i_b > 0, i_c < 0$
2	$i_a > 0, i_b < 0, i_c < 0$	5	$i_a < 0, i_b > 0, i_c > 0$
3	$i_a>0, i_b>0, i_c<0$	6	$i_a < 0, i_b < 0, i_c > 0$

Taking the second current sector and the VV "01 -1 to 000" as an example [DT type: phase A (DT<sub>5</sub>), phase B (DT<sub>1</sub>), phase C (DT<sub>3</sub>), the direction of output current:  $i_a>0$ ,  $i_b<0$ ,  $i_c<0$ ], as shown in Fig. 4, the  $V_{AN}$  is  $0.5V_{dc}$ ,  $V_{BN}$  is  $V_{dc}$ ,  $V_{CN}$  is  $0.5V_{dc}$ , so that the CMV is  $2V_{dc}/3$ , not  $0.5V_{dc}$ , there is a CMV spike.

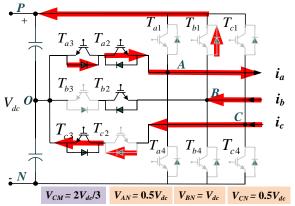


Fig. 4. The converter output phase voltages during DT ( $i_a < 0$ ,  $i_b > 0$ ,  $i_c < 0$ ). To address this CMV spike issue, a novel MPC method, called CMV elimination (CMV-EL), is proposed in [35]: the

candidate VVs are redesigned by pre-excluding the VVs that would cause CMV spikes during the DT from 6MV1Z, only three or five VVs are included to perform optimization in every control period.

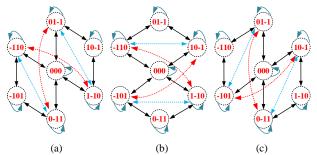


Fig. 5. The candidate vectors of CMV-EL in current sectors. (a) Sectors 1 and 4, (b) Sectors 2 and 5, (c) Sectors 3 and 6.

Although this CMV-EL method could effectively solve the DT problem, it also has the following drawbacks: 1) Due to the insufficient number of VVs used for the current tracking, the phase current THD is poor. 2) The polarity misjudgment of currents during the zero crossing also may cause some CMV spikes.

# III. DEADBEAT MODEL PREDICTIVE CONTROL WITH VIRTUAL VOLTAGE-VECTOR (DB-MPCVV<sup>2</sup>)

# A. Discrete Model of 3LT<sup>2</sup>C Topology with RL Load

To predict the future state of current, a discrete-time model of the  $3LT^2C$  topology with RL load is developed. As shown in Fig. 1, according to Kirchhoff's law, the circuit equation of the  $3LT^2C$  topology with RL load can be derived as follows:

$$\frac{d\mathbf{I}}{dt} = -\frac{R}{L}\mathbf{I} + \frac{V_{dc}}{2L}\mathbf{U} \tag{2}$$

where  $I = [i_a, i_b, i_c]^T$ , represent three-phase inverter output current, U represent the VVs, such as  $[1 -1 \ 0]^T$ ,  $[1 \ 0 \ 1]^T$  in Fig.2. The state-space equation of (2) is expressed as follows:

$$\begin{cases} \mathbf{x}(t) = A\mathbf{x}(t) + B\mathbf{u}(t) \\ \mathbf{y}(t) = C\mathbf{x}(t) \end{cases}$$
 (3)

The state matrix A, input matrix B, and output matrix C in (3) are expressed as follows:

$$\mathbf{A} = \begin{bmatrix} -\frac{R}{L} & 0 & 0\\ 0 & -\frac{R}{L} & 0\\ 0 & 0 & -\frac{R}{L} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} \frac{V_{dc}}{2L} & 0 & 0\\ 0 & \frac{V_{dc}}{2L} & 0\\ 0 & 0 & \frac{V_{dc}}{2L} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1 \end{bmatrix}$$

$$(4)$$

Eq. (3) needs to be discretized by using the Du Hamel formula. Therefore, its discrete-time prediction model can be derived as follows:

$$\begin{cases} x(k+1) = Gx(k) + Hu(k) \\ y(k+1) = Cx(k+1) \end{cases}$$
 (5)

where  $G = e^{AT_s}$ ,  $H = -A^{-1}(I - G)B$ ,  $T_s$  represents the sampling time.

B. Virtual Voltage-Vectors Syntheses and Deadbeat Control

The basic principle of discrete space vector modulation

(DSVM) is that, in each sampling period,  $VV^2s$  can be synthesized by applying several VVs for prefixed time intervals [36]. Therefore, the number of  $VV^2s$  depends on the number of copies divided at each sampling period. If one sampling period is evenly divided into N parts and the switching restrictions between VVs are not considered, the definition of  $VV^2s$  is as follows:

$$V_{vir} = \sum_{i=1,2,3} T_j V_j^{real} \tag{6}$$

Where  $V_i^{real}$  is expressed by

$$V_j^{real} = [V_0, V_1, \dots, V_7], \qquad T_{s1} = \frac{T_s}{N}$$
 (7)

Fig. 6 shows the virtual voltage vector diagram of the  $3LT^2C$ . If N=3, 37 VVs can be synthesized in Fig. 6. It is worth noting that if all 37 VVs are used as candidate vectors, the computational burden will be enormous. Therefore, it is necessary to reduce the number of candidate vectors.

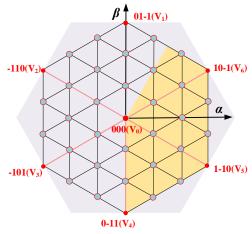


Fig. 6. The virtual voltage vector diagram of the 3LT<sup>2</sup>C.

To facilitate the implementation of the proposed DB-MPCVV<sup>2</sup> method, the VV<sup>2</sup> diagram will be divided by current sector. As shown in Fig. 6, the yellow area is the VVs that can be involved in the first current sector.

Fig. 7 shows the control strategy for the first current sector. As shown in Fig. 7(a), there is a limitation of VV switching in the first and fourth current sector, so the  $VV^2$  synthesis needs to be reconsidered. In Fig.7 (b), since  $V_5$  and  $V_4$  can't be switched with each other, the  $VV^2$ s at  $\mathbf{D}$ ,  $\mathbf{E}$  would not be synthesized. Similarly,  $V_6$  and  $V_0$  can't be switched with each other, so the  $VV^2$  at point  $\mathbf{F}$  can't be synthesized. In addition, the  $VV^2$  synthesis at point  $\mathbf{C}$  could be realized in two schemes:  $[V_4, V_0, V_5]$  and  $[V_5, V_0, V_4]$ . In order to avoid the situation where  $V_4$  and  $V_5$  are adjacent to each other, so the two synthesis schemes need to be adopted alternately with each other.

As shown in Fig. 7(b), the use of  $VV^2s$  would be presented in three cases. ①:The pink area. Since  $VV^2s$  cannot be synthesized at point **D** and **E**, the CMV-EL strategy will be used in this area. ②: The cyan triangular area. When the reference VV stays in this area, the  $VV^2s$  on the three vertices will be used as candidate vectors. ③: The blue trapezoidal area. Since the  $VV^2$  at point **F** cannot be synthesized, the  $VV^2s$  at the four vertices will be used as candidate vectors when the reference VV stays in this area.

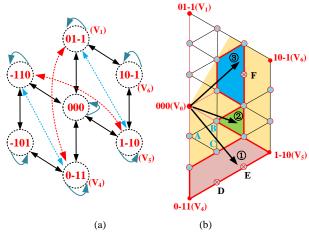


Fig. 7. Control strategy for the first current sector. (a) Candidate vectors in sectors 1 and 4. (b) VV area division in the first current sector.

It is known that control-delay always exists in practical application. To alleviate the delay effects, a simple solution of determining the reference VV at the (k+1)th instant [28] and the reference VV can be obtained as follows:

$$\begin{cases} V_{\alpha}^{*}(k+1) = (R + \frac{L}{T_{s1}})i_{\alpha}^{*}(k+1) - \frac{L}{T_{s1}}i_{\alpha}^{*}(k) \\ V_{\beta}^{*}(k+1) = (R + \frac{L}{T_{s1}})i_{\beta}^{*}(k+1) - \frac{L}{T_{s1}}i_{\beta}^{*}(k) \end{cases}$$
(8)

The reference current  $i_x^*(k+1)$   $(x = \alpha, \beta)$  can be obtained by the Lagrange extrapolation theorem as follows:

$$\begin{cases} i_{\alpha}^{*}(k+1) = 3i_{\alpha}^{*}(k) - 3i_{\alpha}^{*}(k-1) + i_{\alpha}^{*}(k-2) \\ i_{\beta}^{*}(k+1) = 3i_{\beta}^{*}(k) - 3i_{\beta}^{*}(k-1) + i_{\beta}^{*}(k-2) \end{cases}$$
(9)

In this way, the coordinates of the reference VV in the  $\alpha\beta0$ -stationary frame also can be obtained. The coordinates make it possible to know the location of the reference VV and thus select the adjacent vectors in that location. Therefore, the number of candidate vectors is reduced.

To verify the effectiveness of DB strategy in reducing computational burden, four control methods were selected for comparison. This verification is based on MATLAB and the operation is to run the cost function of different control methods 100,000 times, then monitor the calculation time through profiler.

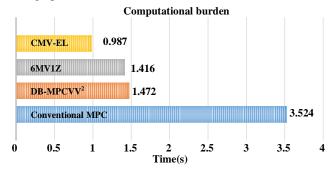


Fig. 8. The comparison of computation burden.

According to the comparison results, it can be seen that DB strategy greatly reduces the computational burden compared to conventional MPC, with a small difference compared to 6MV1Z. Although there is a certain computation gap compared to CMV-EL, the THD performance is another important rating criterion. This would be presented in the simulation and experimental sections.

# C. DB-MPCVV<sup>2</sup> Strategy

As described in cases ② and ③ above, three or four VVs are the optimal candidate VVs when the reference VV stays in the corresponding area. Taking case ② as an example, the  $VV^2$ s of the three vertices of the triangle are  $[V_1,V_5,V_5]$ ,  $[V_0,V_0,V_5]$ ,  $[V_0,V_5,V_5]$ . These three candidate vectors will be evaluated by the cost function, so as to select the most appropriate one. The cost function in this paper is as follows:

$$\begin{cases} x_1 = Gx(k) + HV_{i1} \\ x_2 = Gx_1 + HV_{i2} \\ x(k+1) = Gx_2 + HV_{i3} \\ I(k+1) = y(k+1) = Cx(k+1) \end{cases}$$
(10)

$$g(V_i) = |I(k+1) - I^*(k+1)|^2$$
 (11)

$$V_{best} = \underset{i=1,2,3}{\operatorname{arg\,min}} g(V_i) \tag{12}$$

where  $V_{i1}$ ,  $V_{i2}$ ,  $V_{i3}$  represent the three candidate VVs.  $I^*$  is the reference current.

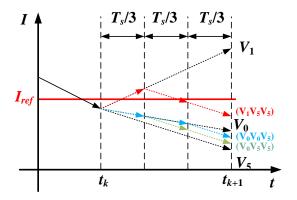


Fig. 9. Current tracking comparison of the conventional MPC and the DB-MPCVV<sup>2</sup>

The current under the action of three  $VV^2s$  is shown in Fig. 9. If only one VV is used in sampling period,  $V_0$  would be the best choice; if use three VVs,  $[V_1, V_5, V_5]$  would be the best choice. Obviously, the use of  $VV^2s$  could help to track the reference current better in one sampling period, so the  $DB-MPCVV^2$  method have a better power quality.

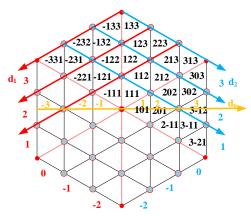


Fig. 10. Area number of VVs.

To identify the area where the reference VV stays in, the area needs to be numbered. As shown in Fig. 10, the yellow axis is divided into six parts  $(d_0: -3, -2, -1, 1, 2, 3)$ . The area between the red lines is labeled as 3,2,1,0,-1,-2  $(d_1)$  and the blue are numbered as 3,2,1,0,-1,-2  $(d_2)$ , so that each area has a coordinate number  $[d_0, d_1, d_2]$ , such as [111], [212], [202] in Fig. 10.

#### D. The 7th Current Sector Control Strategy

The polarity misjudgment of output currents during the zero crossing may result in CMV spiking problems. To solve this problem, the identification method of current sector in [33] is adopted in this paper. As shown in Fig. 11, an additional current sector has been added between the adjacent current sectors, the 7th current sector (1-2, 2-3, 3-4, 4-5, 5-6, 6-1), and the w is the distance from the intersection of the current with the 7th sector to the horizontal axis. The width of the 7th current sector is controlled by w, and the calculation of w can be referred to [33].

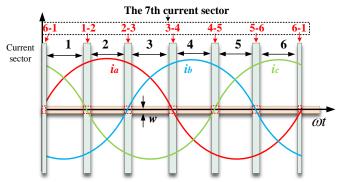


Fig. 11. The 7th current sector.

The current variation per vector acting period on  $\alpha\beta$ 0-stationary frame can be expressed:

$$\begin{cases} \Delta i_{\alpha} = \frac{T_{s1}}{L} (-Ri_{\alpha} + V_{\alpha}) \\ \Delta i_{\beta} = \frac{T_{s1}}{L} (-Ri_{\beta} + V_{\beta}) \end{cases}$$
(13)

where  $T_{s1}$  is the vector acting period,  $\Delta i_{(\alpha)}$  and  $\Delta i_{(\beta)}$  are the current variations.  $V_{(\alpha)}$  and  $V_{(\beta)}$  are the output voltage of  $3LT^2C$ .

$$C\begin{bmatrix} \Delta i_{a} \\ \Delta i_{\beta} \\ \Delta i_{0} \end{bmatrix} = \begin{bmatrix} \Delta i_{a} \\ \Delta i_{b} \\ \Delta i_{c} \end{bmatrix}, C = \frac{3}{2} \begin{bmatrix} \frac{2}{3} & 0 & \frac{2}{3} \\ -\frac{1}{3} & \frac{\sqrt{3}}{3} & \frac{2}{3} \\ -\frac{1}{3} & -\frac{\sqrt{3}}{3} & \frac{2}{3} \end{bmatrix}$$
(14)

Then by using inverse Clarke transform (14) on the  $\alpha\beta\theta$  components, Eq. (13) can be transformed into Eq. (15).

$$\begin{cases} \Delta i_{a} = \frac{T_{s1}}{L} (V_{\alpha} - Ri_{a}) \\ \Delta i_{b} = \frac{T_{s1}}{L} [\frac{1}{2} (-V_{\alpha} + \sqrt{3}V_{\beta}) - Ri_{b}] \\ \Delta i_{c} = \frac{T_{s1}}{L} [\frac{1}{2} (-V_{\alpha} - \sqrt{3}V_{\beta}) - Ri_{c}] \end{cases}$$
(15)

 $V_{(\alpha)}$  and  $V_{(\beta)}$  can be obtained based on coordinate transformation, which are given as:

$$\begin{cases} V_{\alpha} = \frac{2}{3} (V_{a} - \frac{1}{2} V_{b} - \frac{1}{2} V_{c}) \\ V_{\beta} = \frac{2}{3} (\frac{\sqrt{3}}{2} V_{b} - \frac{\sqrt{3}}{2} V_{c}) \end{cases}$$
 (16)

Assuming the DC-link voltage  $V_{dc}$  is 120V and the reference current amplitude i is 6A, so the parameter ranges during the 7th current sector are as follows:

$$\begin{cases} V_x \in [60, 0, -60] \\ i_x \in [5.2, 0, -5.2]_{x=a,b,c} \end{cases}$$
 (17)

As shown in Fig. 7(b), taking the first current sector as an example, when current sector 1-2 is reached, the reference VVs required are 01-1 ( $V_1$ ), 10 -1 ( $V_6$ ), 1-10 ( $V_5$ ). The parameter ranges are as follows:

$$\begin{cases} \left| V_{\alpha} \right| \le 60 \\ \left| -V_{\alpha} + \sqrt{3}V_{\beta} \right| \le 120 \\ \left| -V_{\alpha} - \sqrt{3}V_{\beta} \right| \le 120 \end{cases}$$
 (18)

According to Eq. (15), where  $T_{s1}$ =20 $\mu$ s, R=5 $\Omega$ , L=12mH, then the  $\Delta i_{(x=a,b,c)}$  max can be calculated as 0.143A. w should be larger than  $\Delta i_{(x)}$ max, so that w could be chosen as 0.15 A.

The VV<sup>2</sup>s are used in the first to sixth current sectors, while a new control method is required in the 7th current sector. As shown in Fig. 12, there are same vector switching between Figs. a and b, just as shown in circles of the same color, so these vectors can be used in 1-2 and 4-5 current sector. Similarly, vectors that are available for the 7th current sector are summarized in Table IV.

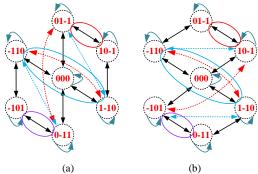


Fig. 12. Available candidate vectors in sectors 1-2 and sectors 4-5.

# E. Implementation

The control block diagram of the DB-MPCVV<sup>2</sup> method is shown in Fig. 13. To compensate the delay effects, a delay compensation algorithm in [33] can be used as follows:

$$\begin{cases} i_{\alpha}(k+1) = \cos\phi i_{\alpha}(k) - \sin\phi i_{\beta}(k) \\ i_{\beta}(k+1) = \sin\phi i_{\alpha}(k) + \cos\phi i_{\beta}(k) \end{cases}$$
(19)

where  $\Phi = \omega T_{s1}$ ,  $\omega$  is the output angular frequency of the inverter, and  $T_{s1}$  is the vector acting period.

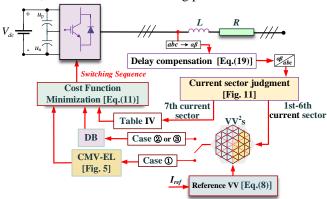


Fig. 13. Control block diagram of the DB-MPCVV<sup>2</sup>.

At the beginning, the proposed DB-MPCVV<sup>2</sup> method requires a judgment of current sector. If it is the 1st-6th current sectors: the reference VV position is used to determine which case it belongs to, and then CMV-EL method or DB control is implemented. For the 7th current vector, the candidate vectors in Table IV would be used. Finally, the cost function selects the optimal switching sequence.

TABLE IV

Available Candidate Vectors in the 7th Current Sector

7th Sect	tor Ave	ailable vector sv	vitching
1-2, 4-5	-110, 000, 1-10	01-1, 10-1	-101, 0-11
2-3, 5-6	10-1, 000, -101	-110, 01-1	0-11, 1-10
6-1, 3-4	01-1, 000, 0-11	-110, -101	10-1, 1-10

#### IV. SIMULATION VERIFICATION

To verify the effectiveness of the proposed DB-MPCVV<sup>2</sup> method and observe the CMV performance, a simulation model is built based on MATLAB/Simulink and the DC-link voltage ( $V_{dc}$ ), sampling time ( $T_s$ ) and dead-time are set to 120 V, 60  $\mu s$  and 2  $\mu s$ , respectively.

# A. DB-MPCVV<sup>2</sup> Method with Different Loads

Fig. 14 shows the simulation results of the three-phase current, THD and CMV with different loads and the three cases in Fig.7 are also included. Overall, it can be seen that the CMV can be maintained at a constant 60V ( $V_{dc}/2$ ) when different loads are used.

Figs. 14 (a), (b) and (d) [case ② and ③] are the results of DB method and their THDs are maintained at around 1.5%, 1.4%, and 0.7%. Furthermore, there are some varying degrees of fluctuations on their THD values. This is because the 7th current sector is added to the proposed method, fewer available vectors in the 7th current sector result in a large difference between the reference VV and the candidate VV, and this difference is related to the load. Therefore, the THD values of a, b fluctuates greatly, and the THD of d is relatively stable. It is worth noting that the CMV-EL method is used in c [case ①] and fewer candidate VVs make its THD value fluctuation large.

In summary, the proposed DB-MPCVV<sup>2</sup> method uses two control methods considering vector area division, thus enabling control over the full range of modulation index. Although the output current THD fluctuates, it is still at a low level. And this DB-MPCVV<sup>2</sup> method also could achieve constant CMV when use different loads.

# B. Current THD and Predicted Current Error

1) THD Comparison with Different Load Frequency and Current: Same load (L:12mH, R:5Ω) is considered for the proposed DB-MPCVV² method and the existing control method for comparison. The current THD values are shown in Fig. 15 for various output frequency with four control methods. It can be observed that CMV-EL and 6MV1Z with fewer candidate vectors have higher THD values, while conventional MPC with more candidate vectors has smaller THD values. In addition, VV²s could enhance the current tracking capability of control method, so that the proposed DB-MPCVV² greatly reduces THD, and even outperforms conventional MPC at 30, 40, 60 Hz.

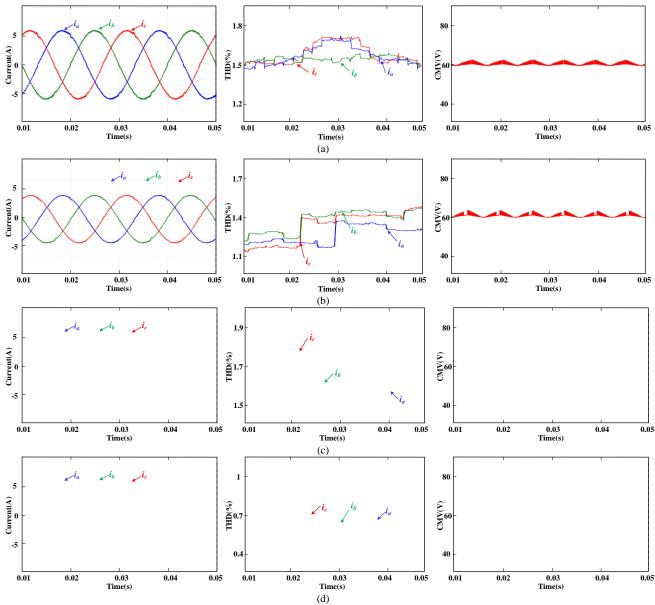


Fig. 14. Simulation results of the three-phase current, THD and CMV with different loads. (a) L:10mH,  $R:5\Omega$ . (b) L:13mH,  $R:5\Omega$ . (c) L:20mH,  $R:5\Omega$ . (d) L:30mH,  $R:2\Omega$ .

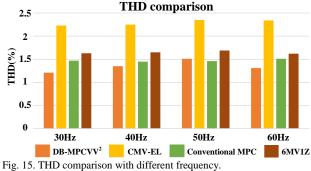


Fig. 16 shows the THD comparison of four control methods under different load currents. Similarly, the proposed DB-MPCVV $^2$  method has the lowest THD value. In conclusion, the proposed method has good power quality for different magnitudes and frequencies of the output current.

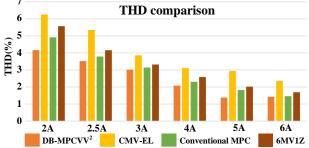


Fig. 16. THD comparison with different load current.

2) Current Error Comparison: Fig. 17 shows the percentages of the current errors obtained by using four control methods. The error expression in [37] of the current error is defined as the absolute difference between the load and reference currents normalized to the respective rms value of the load current references as:

$$Error(\%) = \frac{\frac{1}{N} \sum_{q=a,b,c} \sum_{k=1}^{N} |i_q(k) - i_q^*(k)|}{\sum_{q=a,b,c} RMS(i_q^*(k))} \times 100\%$$
 (20)

where the N is 20000, per fundamental period of the current.  $i_q(k)$  and  $i_q^*(k)$  are the kth instant load and reference current.

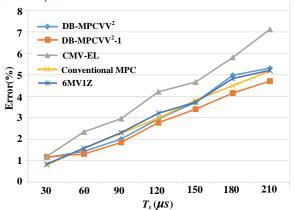


Fig. 17. Current errors comparison.

Compared with 6MV1Z and conventional MPC, the DB-MPCVV² has little difference in current error and it may be observed that the DB-MPCVV² method yields slightly higher current errors than the conventional MPC within 150µs to 210µs. An explanation of this is as follows: The VV action time in the 7th sector is one sampling period (1s), unlike the VV²s which act on 1/3 of the sampling period, this would result in a significant difference between the candidate VV and the reference VV, as shown in Fig. 18. If the vector action time in the 7th sector is reduced by half (0.5s), the difference will decrease, thereby enhancing the current tracking ability, just like DB-MPCVV²-1 in Fig.17.

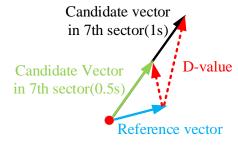


Fig. 18. Action time improvement of the candidate vector.

# V. EXPERIMENTAL VERIFICATION

#### A. Hardware Setup

To observe the steady- and dynamic-state performance of proposed DB-MPCVV $^2$  method, experimental verifications are given on a hardware prototype of a three-phase  $3LT^2C$  converter in the laboratory. The hardware setup is shown in Fig. 19.



Fig. 19. Experimental setup and designed converter.

TABLE V PARAMETER SPECIFICATION

Parameter	Description	Values
$V_{dc}(V)$	DC-link voltage	120
$f_{\rm g}({\rm Hz})$	Frequency	50
$C_{dc}(mF)$	DC-link capacitance	2
L(mH)	Inductance	12
$R(\Omega)$	Resistance	5
N	DSVM parts	3
$T_s(\mu s)$	Sampling time	90
$T_d(\mu s)$	Dead time	2

The control strategy is referenced by Fig. 13 and it is implemented on a 32-bit float-point digital signal processor (DSP-TMS320F28335, Texas Instruments). The 3LT<sup>2</sup>C converter consists of six 1MBH50D-060 (600V/50A) IGBTs and six 2MBI150U2A-060 (600 V/150 A) IGBTs for vertical and horizontal bridges from FUZI company. A high-precision series voltage divider and a full differential isolation amplifier OPA4340 are used to measure the current and CMV. The parameters are shown in Table V.

The experiment is performed mainly with two purposes.

1) Compare the steady-state CMV and THD performance with existing methods. 2) Compare the dynamic response and CMV performance with existing control methods when the amplitude and frequency of the load current change.

# B. Steady-State Performance

Figs. 20 and 21 depict the steady-state performance of the three-phase current and CMV by using four control methods. As shown in Figs.20 (a) and (c), the THDs of CMV-EL and 6MV1Z are 3.74% and 2.54%. These two methods obtain constant CMVs by selecting specific vectors, thus resulting in a significant reduction in candidate vectors. Therefore, the current THD value is high. The conventional MPC has sufficient candidate vectors, so its THD value is only 2.17%. In Fig.21, due to ignoring the DT effect, the CMV of 6MV1Z did not remain constant and there were some  $V_{dc}/6$ CMV variation, like conventional MPC. Moreover, there is a misjudgment of current polarity in CMV-EL, so some CMV spikes (red dashed ellipse) were presented in Fig.21 (a). Regarding the proposed DB-MPCVV<sup>2</sup>, the CMV remains constant due to the addition of the 7th current sector. In addition, the VV2s which are synthesized by actual vectors are used to reduce the current THD to 2.28%.

In summary, the proposed DB-MPCVV<sup>2</sup> method is able to achieve constant CMV while obtaining a better current power quality in steady-state.

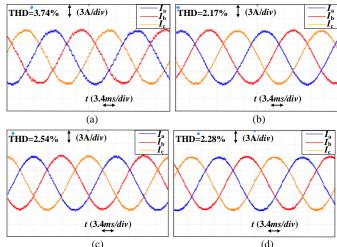


Fig. 20. Steady-state performance of the load current (50 Hz). (a) CMV-EL. (b) Conventional MPC. (c) 6MV1Z. (d) DB-MPCVV<sup>2</sup>.

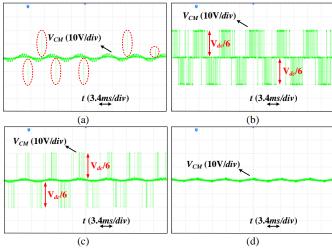
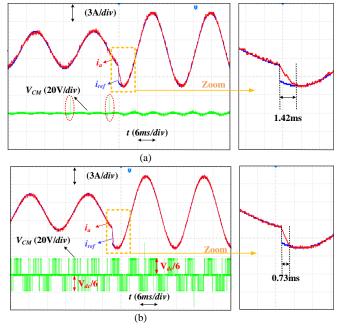


Fig.21. Steady-state performance of CMV. (a) CMV-EL. (b) Conventional MPC. (c) 6MV1Z. (d) DB-MPCVV<sup>2</sup>.

# C. Dynamic Performance

1) Dynamic Response of the Load Current: Fig. 22 depicts the dynamic process of load current changing from 3 to 6A. From the CMV experimental results, it can be seen that the proposed DB-MPCVV² remains constant, while the CMV-EL also exhibits some slight CMV spikes, and conventional MPC have V<sub>dc</sub>/6 CMV variation. In terms of current dynamic response, conventional MPC has a response time of 0.73 ms due to its sufficient candidate vectors, while 6MV1Z and CMV-EL have the response time of 0.92 and 1.42 ms, respectively. It is worth noting that the proposed DB-MPCVV² has the slowest current response (2.03ms), which is mainly caused by the use of DB control. The explanation is as follows:

Taking a sector as an example [see Fig. 23 (a)], when the load current is increased by using the DB control, the reference VV would shift from area B to area A. However, the candidate vectors in area A could only make the current changes according to the slope of the Change-point [see Fig. 23 (b)]. Therefore, compared to other MPCs that can freely choose vectors, the dynamic response time of DB-MPCVV² would be longer.



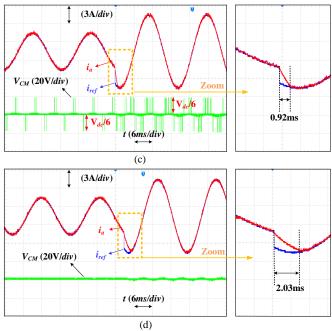


Fig. 22. Dynamic response process of the load current from 3 to 6A. (a) CMV-EL. (b) Conventional MPC. (c) 6MV1Z. (d)  $DB-MPCVV^2$ .

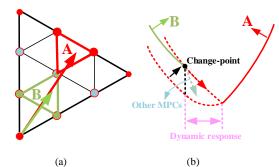


Fig. 23. The dynamic response of DB-MPCVV.

2) Dynamic Response of the Load Frequency: Fig. 24 shows that the CMV and dynamic process of the reference current has a step change in the frequency from 30 to 60 Hz. From the experimental results of current tracking, it can be obviously observed that the current controlled by the proposed DB-MPCVV² follow the reference current change as fast as those controlled by the conventional method for step changes. In addition, the CMV of proposed DB-MPCVV² also could keep constant in the dynamic process of frequency change. In terms of power quality, the THD performance of the four methods at 30 Hz are 3.34%, 2.24%, 2.53% and 1.85% respectively, while the THD performance at 60 Hz are 3.72%, 2.28%, 2.38% and 2.02%, respectively. It can be seen that the proposed DB-MPCVV² has good power quality in both cases.

In conclusion, the proposed DB-MPCVV<sup>2</sup> method still has good power quality and constant CMV during the dynamic process. Furthermore, it is also need to note that the use of DB control reduces the computational burden but this also increases the dynamic time response and a good solution should be defined as a compromise between the two.

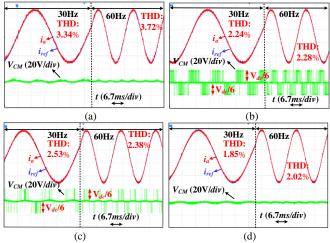


Fig. 24. Dynamic response of the frequency from 30 to 60Hz. (a) CMV-EL. (b) Conventional MPC. (c) 6MV1Z. (d) DB-MPCVV<sup>2</sup>.

# VI. CONCLUSION

In this article, a DB-MPCVV<sup>2</sup> control method for 3LT<sup>2</sup>C topology is proposed to achieve constant CMV and improve power quality. By analyzing the vector switching in the current sector considering DT effect, the proposed DB-MPCVV<sup>2</sup> establishes VV<sup>2</sup>s, thereby improving the power quality of the load current. And the DB control is introduced in this paper to solve the high computational burden caused by VV<sup>2</sup>s. Moreover, a unique the 7th current sector control is used in DB-MPCVV<sup>2</sup> to solve the CMV spiking problem caused by current polarity misjudgment. The simulation results show that the DB-MPCVV<sup>2</sup> method could maintain constant CMV under various loads. In addition, the good power quality of the DB-MPCVV<sup>2</sup> method under different current magnitudes and frequencies is also verified. The experimental results demonstrate the effectiveness of the proposed DB-MPCVV<sup>2</sup> by comparing it with the existing methods from both steady-state and dynamic aspects. It is suggested the proposed method be applied to motor drive or PV grid-connected system in future work.

#### REFERENCES

- T. Cao, Y. Yu, J. Zhang, J. Rodriguez, K. T. Chong, and B. Long, "Pseudo-Three-Layer Sequential Model-Free Predictive Control With Neural-Network Observer for Parallel T-Type Three-Level Converters," *IEEE Transactions on Power Electronics*, vol. 39, no. 7, pp. 7848-7862, 2024.
- [2] B. Long et al., "Noninteger Lexicographic-Optimization-Based Sequential Model-Predictive Fault-Tolerant Control of T-Type Shunt Active Power Filter," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 7169-7184, 2022.
- [3] B. Long, T. Cao, D. Sheng, J. Rodriguez, J. M. Guerrero, and K. T. Chong, "Sequential Model Predictive Fault-Tolerance Control for T-Type Three-Level Grid-Connected Converters With LCL Filters," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 9, pp. 9039-9051, 2022.
- [4] B. Long, C. Hu, Z. Chen, J. Hu, J. Rodríguez, and X. Zang, "Fractional-Order Sequential Model Predictive Control of Three-Phase Fractional-Order T-Type Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 6, pp. 5820-5832, 2023.
- [5] X. Wang, J. Hu, C. Garcia, J. Rodriguez, and B. Long, "Robust Sequential Model-Free Predictive Control of a Three-Level T-Type Shunt Active Power Filter," *IEEE Transactions on Power Electronics*, vol. 39, no. 8, pp. 9505-9517, 2024.
- [6] D. Karwatzki and A. Mertens, "Generalized Control Approach for a Class of Modular Multilevel Converter Topologies," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 2888-2900, 2018.
- [7] E. Lorenzani, G. Migliazza, F. Immovilli, C. Bianchini, and G. Buticchi, "Ground leakage current in PV three-phase current source

- inverter topologies," in *IECON 2017 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, pp. 4221-4226.
- [8] X. Guo, J. Zhou, R. He, X. Jia, and C. A. Rojas, "Leakage Current Attenuation of a Three-Phase Cascaded Inverter for Transformerless Grid-Connected PV Systems," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 676-686, 2018.
- [9] Y. Ma, J. Gong, D. Jiang, Z. Liu, X. Zhao, and R. Qu, "A Universal Common Mode Voltage Suppression Algorithm for AC Motors with Odd Phase Number," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1-1, 2024.
- [10] Z. Zeng and S. M. Goetz, "A Zero Common Mode Voltage PWM Scheme with Minimum Zero-Sequence Circulating Current for Two-Parallel Three-Phase Two-Level Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1-1, 2024.
- [11] Z. Y. Rui Chen, and Wenhui Zhang, "Adaptive Fuzzy Sliding Mode Control for Nonlinear Systems with Unknown Dead-zone," *IAENG International Journal of Applied Mathematics*, vol. 54, no. 12, pp. 2588-2595, 2024.
- [12] Y. Y. Yuntian Ding, Zhilian Yan, and Weipeng Tai, "Robust Control for Uncertain Discrete-Time Linear Systems Using Reinforcement Learning With Discount Factor," *IAENG International Journal of Applied Mathematics*, vol. 54, no. 12, pp. 2783-2791, 2024.
- [13] a. S. C. R. Vineetha G.R, "Enhancing Facility Layout Optimization: A Performance Analysis of Genetic Algorithm Variants in Dynamic Facility Layout Problems," *IAENG International Journal of Computer Science*, vol. 51, no. 11, pp. 1898-1913, 2024.
- [14] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4537-4551, 2015.
- [15] S. Takahashi, S. Ogasawara, M. Takemoto, K. Orikawa, M. J. t. I. C. o. E. M. Tamate, and Systems, "Common-mode voltage attenuation of an active common-mode filter in a motor drive system fed by a PWM inverter," pp. 1-6, 2019.
- [16] X. Guo, "Three-Phase CH7 Inverter With a New Space Vector Modulation to Reduce Leakage Current for Transformerless Photovoltaic Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 708-712, 2017.
- [17] T. K. S. Freddy, N. A. Rahim, W.-P. Hew, and H. S. Che, "Modulation Techniques to Reduce Leakage Current in Three-Phase Transformerless H7 Photovoltaic Inverter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 322-331, 2015.
- [18] A. Hota and V. Agarwal, "A New H8 Inverter Topology With Low Common Mode Voltage and Phase Current THD for 3- Induction Motor Drive Applications," *IEEE Transactions on Industry Applications*, vol. 58, no. 5, pp. 6245-6252, 2022.
- [19] H. Ma, Z. Lan, and Z. Chen, "Non-isolated H10 three-phase inverter for leakage current suppression," *Journal of Power Electronics*, vol. 20, no. 5, pp. 1139-1148, 2020/09/01 2020.
- [20] R. Rahimi, S. Farhangi, B. Farhangi, G. R. Moradi, E. Afshari, and F. Blaabjerg, "H8 Inverter to Reduce Leakage Current in Transformerless Three-Phase Grid-Connected Photovoltaic systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 910-918, 2018.
- [21] Y. Xiang, X. Pei, M. Wang, P. Shi, and Y. Kang, "An Improved H8 Topology for Common-Mode Voltage Reduction," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5352-5361, 2019.
- [22] L. Concari, D. Barater, G. Buticchi, C. Concari, and M. Liserre, "H8 Inverter for Common-Mode Voltage Reduction in Electric Drives," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4010-4019, 2016.
- [23] T. D. Duong, M. K. Nguyen, T. T. Tran, D. V. Vo, Y. C. Lim, and J. H. Choi, "Three-Phase Impedance-Source Inverter With Common-Mode Voltage Reduction," *IEEE Access*, vol. 9, pp. 164510-164519, 2021.
- [24] T. T. Tran et al., "A Three-Phase Constant Common-Mode Voltage Inverter With Triple Voltage Boost for Transformerless Photovoltaic System," *IEEE Access*, vol. 8, pp. 166692-166702, 2020.
- [25] A. A. Khan, N. A. Zaffar, M. J. Ikram, Y. Wu, and L. Peretti, "Combined Reduction of DC-link Harmonics and Common Mode Voltage in Interleaved Multi-inverter Systems by Modified SVPWM Schemes," *IEEE Transactions on Industrial Electronics*, pp. 1-11, 2024
- [26] M. C. Cavalcanti, A. M. Farias, K. C. Oliveira, F. A. S. Neves, and J. L. Afonso, "Eliminating Leakage Currents in Neutral Point Clamped Inverters for Photovoltaic Systems," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 435-443, 2012.
- [27] S. Xia, X. Wu, J. Zheng, X. Li, and K. Wang, "A Virtual Space Vector PWM With Active Neutral Point Voltage Control and Common Mode

- Voltage Suppression for Three-Level NPC Converters," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 12, pp. 11761-11771, 2021.
- [28] M. Akbari, S. A. Davari, R. Ghandehari, F. Flores-Bahamonde, and J. Rodriguez, "Reduction of Calculations Virtual Voltage Vectors-based Predictive Control for 3-Level NPC Inverters with Constant Common-Mode Voltage," in 2023 IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE), 2023, pp. 1-6.
- [29] a. B. P. P. Aengchuan, "A Comparative Study of Design of Experiments and Fuzzy Inference System for Plaster Process Control," in Lecture Notes in Engineering and Computer Science: Proceedings of The World Congress on Engineering, London, U.K., 2017, pp. 184-188.
- [30] W.-S. Jeong, S.-H. Kim, J. Yi, and C.-Y. Won, "Finite Control Set—Model Predictive Control of H8 Inverter Considering Dead-Time Effect for PMSM Drive Systems With Reduced Conducted Common-Mode EMI and Current Distortions," *IEEE Transactions on Power Electronics*, vol. 37, no. 5, pp. 5342-5356, 2022.
- [31] X. Wang et al., "Common-mode voltage elimination of three-level T-type inverters with a finite control set model predictive control method," in 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), 2018, pp. 992-997.
- [32] S. Kwak and S. Mun, "Common-mode voltage mitigation with a predictive control method considering dead time effects of three-phase voltage source inverters," *IET Power Electronics*, vol. 8, no. 9, pp. 1690-1700, 2015/09/01 2015.
- [33] L. Guo, N. Jin, C. Gan, L. Xu, and Q. Wang, "An Improved Model Predictive Control Strategy to Reduce Common-Mode Voltage for Two-Level Voltage Source Inverters Considering Dead-Time Effects," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3561-3572, 2019.
- [34] L. Guo, N. Jin, C. Gan, and K. Luo, "Hybrid Voltage Vector Preselection-Based Model Predictive Control for Two-Level Voltage Source Inverters to Reduce the Common-Mode Voltage," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 4680-4691, 2020.
- [35] X. Wang, J. Zou, Z. Dong, C. Xie, K. Li, and M. Guerrero Josep, "Novel Model Predictive Control Method to Eliminate Common-mode Voltage for Three-level T-type Inverters Considering Dead-time Effects," (in En), *Journal of Power Electronics*, vol. 18, no. 5, pp. 1458-1469, 09/20 2018.
- [36] D. Casadei, G. Serra, and K. Tani, "Implementation of a direct control algorithm for induction motors based on discrete space vector modulation," *IEEE Transactions on Power Electronics*, vol. 15, no. 4, pp. 769-777, 2000.
- [37] S. Kwak and S. k. Mun, "Model Predictive Control Methods to Reduce Common-Mode Voltage for Three-Phase Voltage Source Inverters," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 5019-5035, 2015.