# Two-Quadrant Current-Mode Logarithmic and Anti-logarithmic Amplifiers with Temperature Compensation

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***Abstract*—This paper proposes circuit topologies for realizing two-quadrant current-mode logarithmic and anti logarithmic amplifier configurations with temperature compensation. The design approach employs the translinear approach to generate the output currents that directly correspond to the absolute values of the logarithmic and anti logarithmic functions. The proposed circuits can operate at a low-level supply voltage of 2V with both input and output current signals. A detailed examination of the non-ideal circuit performance has also been considered. To validate their functionality and illustrate their superior thermal stability, the developed circuits have been simulated. All simulations were conducted via PSPICE for a real bipolar transistor model of the HFA3096 technology.**

***Index Terms*—current-mode circuit, logarithmic amplifier, anti-logarithmic amplifier, temperature compensation, translinear circuit**

## I. INTRODUCTION

THE operational idea of a logarithmic (LOG) amplifier is to provide an output voltage that is proportionate to the logarithm of the input voltage. It converts a wide range of input voltage levels into a significantly smaller range of output levels, making it advantageous for applications where an extensive dynamic range is required. Conversely, the anti-logarithmic (ALOG) amplifier generates an output voltage that is proportional to the exponential function of the input voltage. The exponential function transforms a limited range of input voltage levels into a significantly wider range of output levels, providing it beneficial for solution needing high voltage gain [1]-[2]. The specialized circuits in amplifiers convert a wide dynamic range of input signals into a correspondingly smaller or larger dynamic range of output signals. LOG and ALOG amplifier circuits are utilized in extensive analog data compression and expansion applications. The applications of LOG and ALOG amplifiers are numerous and diverse. They are utilized in radio communications to measure the radio signal strength, in audio systems to regulate sound loudness, and in photonics to quantify light intensity. These amplifiers are frequently utilized in scientific instruments, such as oscilloscopes, to present signals in a logarithmic format, facilitating the observation and analysis of signals that encompass a broad spectrum of values. Additionally, numerous applications include the linearization of output transducers, slide rule analog computation, control of time-variable gain in sonar systems, and the automated gain control approach.

Recently, a companding current-mode (CM) technique, also known as log-domain filtering, was initially suggested in [3]. This technique compresses the input signal prior to processing and then expands it [4], and has been extensively utilized in many applications and solutions [5]-[8]. Consequently, the LOG and ALOG amplifiers have become essential foundational components for this approach. Despite the development of several log-domain filtering approaches in [8]-[11], a significant limitation of all available circuits is their considerable dependence on absolute temperature. Therefore, certain temperature compensated methodologies are necessary. Several techniques are utilized to alleviate variation in temperature in LOG and ALOG amplifier circuits; nonetheless, these circuits often operate only in one quadrant [12].

To address the aforementioned limitations, this paper mainly presents innovative two-quadrant LOG and ALOG current amplifier circuits with inherent temperature compensation. By leveraging the translinear principle in combination with CM signal processing, the proposed circuits overcome conventional single-quadrant operation constraints and offer enhanced thermal stability over a wide temperature range. Furthermore, the designs achieve full CM functionality, enabling seamless integration into modern analog processing systems with minimal power supply requirements. The contributions of this work are threefold: (1) the development of temperature-insensitive LOG and ALOG amplifiers that operate in two quadrants; (2) the realization of electronically tunable gain characteristics through external bias control; and (3) the verification of

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circuit performance using practical PSPICE simulations based on the HFA3096 mixed bipolar array process. These characteristics collectively establish the proposed circuits as efficient and versatile solutions for advanced analog signal processing applications.

## II. Fundamental Functional Blocks

This section describes the basic circuit functional blocks utilized in the design and synthesis of the proposed two quadrant CM LOG and ALOG amplifier circuits.

### A. *Absolute-current-value circuit*

Fig. 1 shows the absolute-current-value circuit, which generates an output current $I_{o1}$ proportional to the absolute value of an input signal current $I_{in}$. In this circuit, the two series diodes, comprising transistors $Q_6$ and $Q_7$, provide a bias voltage equal to $2V_{BE}$ at the base of $Q_5$. Due to this biased configuration, the Darlington pair consisting of $Q_4$ and $Q_5$, along with transistor $Q_1$ will not conduct at the same time.

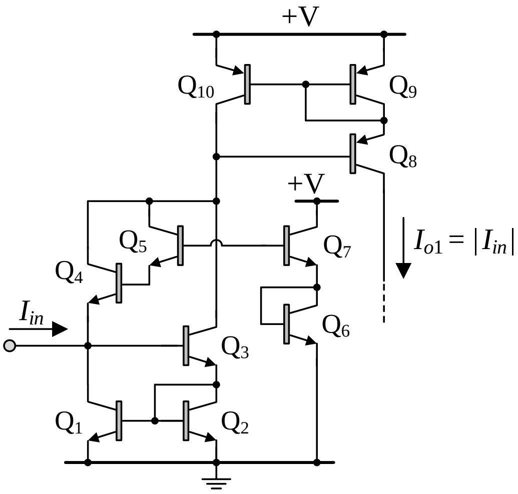



Fig. 1. Absolute-current-value circuit.

When $I_{in}$ is positive (entering the circuit), the Darlington pair is inactive, and the current $I_{in}$ flows through $Q_1$, which is part of a Wilson current mirror formed by $Q_1$, $Q_2$, and $Q_3$. The Wilson current mirror $Q_8$-$Q_{10}$ will transfer the input current $I_{in}$ to the output current $I_{o1}$. Consequently, the output current $I_{o1}$ is given by: $I_{o1} = I_{in}$. For $I_{in}$ negative, the Wilson current mirror $Q_1$-$Q_3$ is turned off, and the current $I_{in}$ passes through the Darlington pair $Q_4$-$Q_5$. It is evident that $I_{o1}$ equals $I_{in}$, or $I_{o1} = I_{in}$. From circuit operation, the relationship between $I_{in}$ and $I_{o1}$ can then be expressed as:

$$I_{o1} = |I_{in}| \quad . \tag{1}$$

### B. *Current multiplier/divider circuit*

The fundamental scheme for a npn current mirror with controlled gain is illustrated in Fig. 2. In this scheme, transistors $Q_1$-$Q_4$ serve as a classical Seevinck translinear based current multiplier/divider circuit [13]. The fundamental scheme for a npn current mirror with controlled gain is illustrated in Fig. 2. If the common-emitter current gain ($\beta$) of transistor is significantly greater than unity, the output current $I_4$ can be precisely given by:

$$I_4 = \frac{I_1 I_2}{I_3} \quad . \tag{2}$$

The circuit clearly has the ability to function as a CM multiplier/divider. In this instance, the circuit may utilize any one of the three currents ($I_1$, $I_2$, and $I_3$) as input.

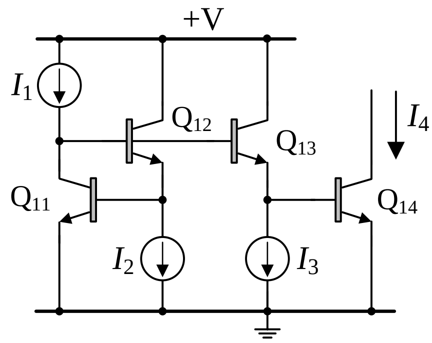



Fig. 2. Translinear-based current multiplier/divider circuit.

### C. *Temperature-dependent LOG current amplifier*

Fig. 3 shows a circuit diagram of a CM LOG amplifier [12]. This configuration slightly modifies the current multiplier/divider circuit depicted in Fig. 2 by adding transistor $Q_{18}$ and resistors $R_1$ and $R_2$. Neglecting base currents and setting $R = R_1 = R_2$, the following relationship is obtained based on the translinear principle:

$$I_{o2} = \left(\frac{V_T}{R}\right) \ln\left(\frac{I_A}{I_B}\right) \quad , \tag{3}$$

where $I_A$ and $I_B$ are the external DC bias currents and $V_T$ is the usual thermal voltage. At room temperature, $V_T$ is defined as $kT/q$, approximately 26 mV, which is directly dependent on the absolute temperature $T$. Equation (3) explicitly indicates that the circuit can produce a LOG function output current; nonetheless, its main constraint relates strongly with ambient temperature. Note that in order to achieve $I_{o2} \geq 0$, the condition $I_A \geq I_B$ must be satisfied.

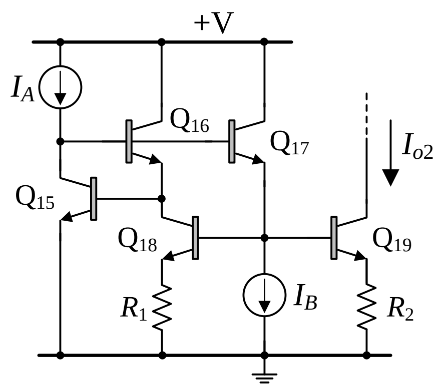



Fig. 3. Temperature-dependent LOG current amplifier.

### D. *Temperature-dependent ALOG current amplifier*

Fig. 4 shows the translinear-based temperature-dependent ALOG current amplifier circuit [12]. By applying the translinear concept, we can derive the output current $I_{o3}$ as:

$$I_{o3} = I_C e^{\left(\frac{I_D R_3}{V_T}\right)} \quad . \tag{4}$$

Now, the output current of the circuit shown in Fig. 4 is characterized by an ALOG function that is significantly influenced by the usual thermal voltage $V_T$.

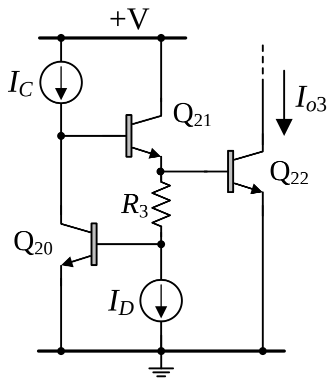
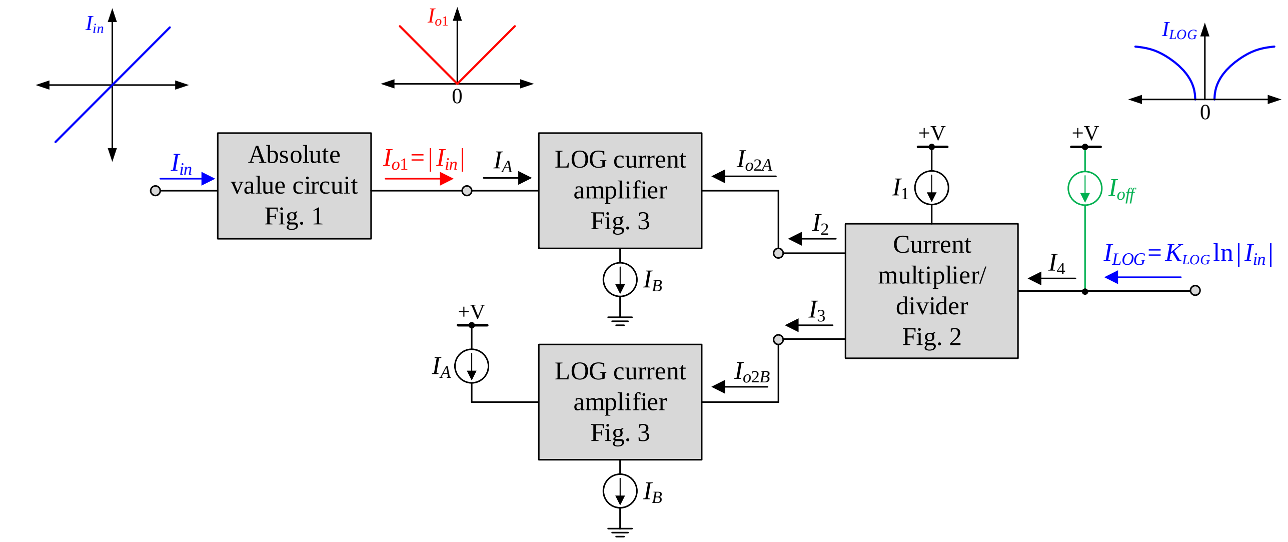



Fig. 4.  Temperature-dependent ALOG current amplifier.

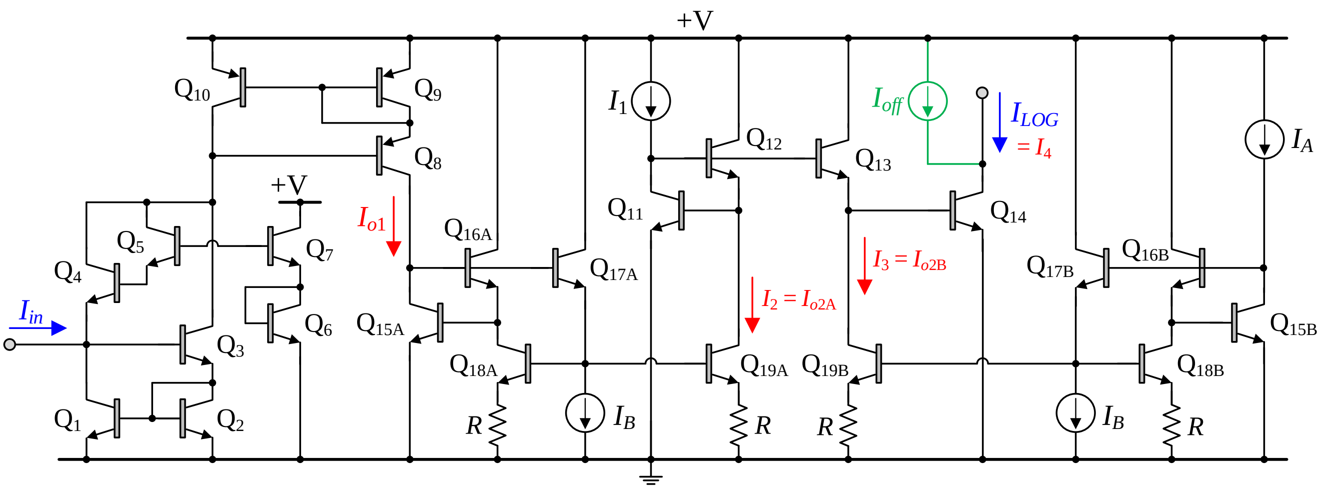
In the following, we will introduce the two-quadrant LOG and ALOG function generator circuits with temperature compensation, which are realized from the functional circuit blocks described in Figs. 1-4.

## III. Proposed Two-Quadrant Logarithmic Current Amplifier

This section discusses the circuit configuration for implementing a two-quadrant CM LOG amplifier circuit with temperature compensation. In Fig. 5(a), the concept of the proposed two-quadrant LOG current amplifier is demonstrated. By combining an absolute-value circuit followed by temperature-dependent LOG current amplifiers and the current multiplier/divider circuit, we can realize a temperature-insensitive LOG function current generator that can operate in two quadrants. Fig. 5(b) shows the practical transistor realization of the proposed temperature-insensitive two-quadrant LOG current amplifier.




(a)




(b)

Fig. 5.  Proposed two-quadrant current-mode LOG amplifier with temperature compensation.
(a) principle block diagram        (b) transistor-level circuit

Since the temperature-dependent LOG current amplifier shown in Fig. 3 constitutes the primary section of the circuit in Fig. 5(b), we can express the currents $I_2$ and $I_3$ as LOG functions that are directly proportional to the thermal voltage $V_T$ as follows:

$$I_2 = I_{o2A} = \left(\frac{V_T}{R}\right)\ln\left(\frac{|I_{in}|}{I_B}\right) , \quad (5)$$

and

$$I_3 = I_{o2B} = \left(\frac{V_T}{R}\right)\ln\left(\frac{I_A}{I_B}\right) . \quad (6)$$

Considering the current multiplier/divider $Q_{11}$-$Q_{14}$, we can get the output LOG current $I_{LOG}$ of the circuit by substituting $I_2$ and $I_3$ from (5) and (6) into (2) as follows:

$$I_{LOG} = \left(\frac{I_1}{K_1}\right)\ln\left(\frac{|I_{in}|}{I_B}\right) , \quad (7)$$

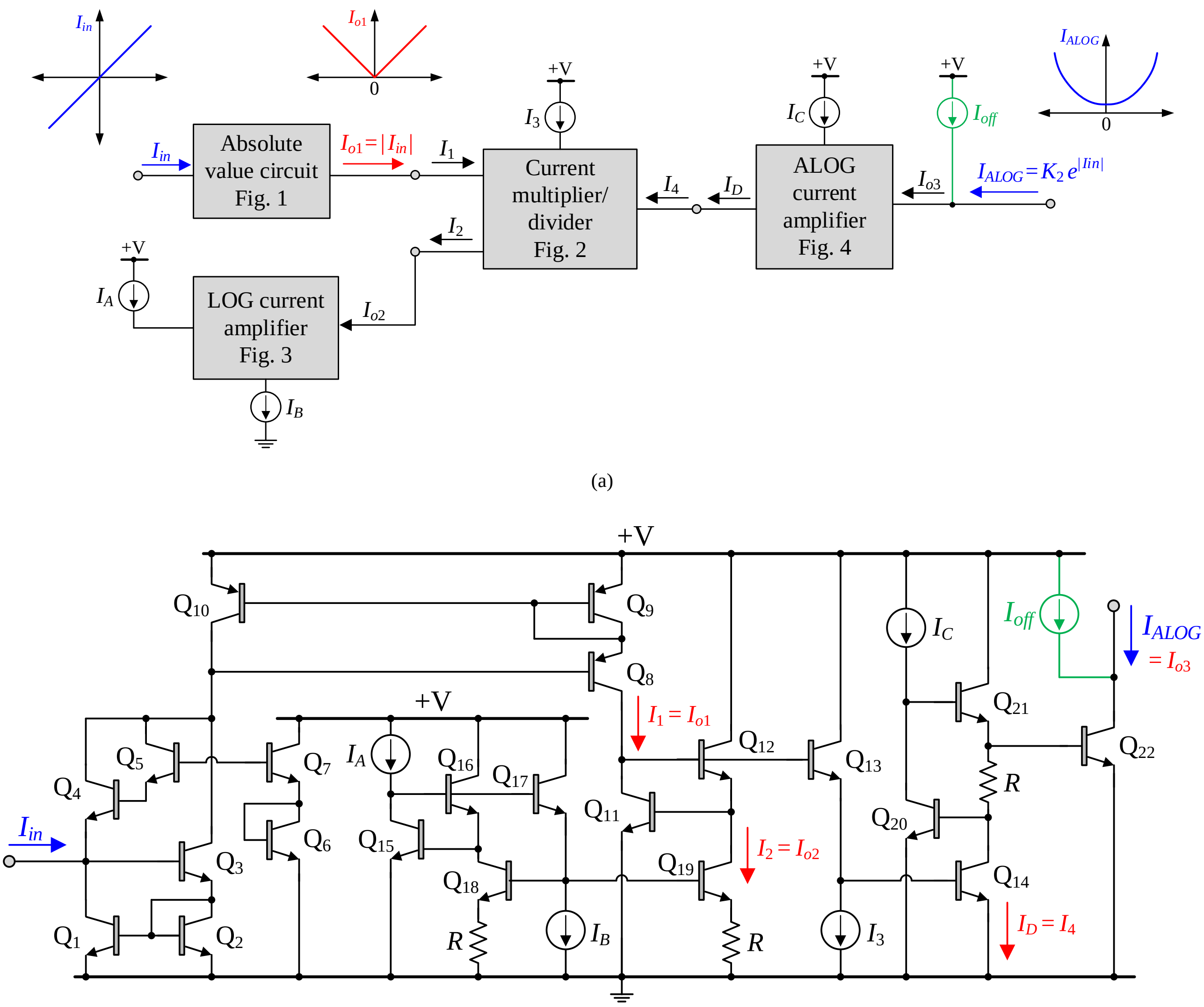
where

$$K_1 = \ln\left(\frac{I_A}{I_B}\right) . \quad (8)$$

As stated in (7) and (8), the proposed circuit shown in Fig. 3 produces a logarithmic function current generator with the transfer current gain of $I_1/K_1$. It is important to note that the output current and its transfer gain are only determined by the externally supplied currents and are not significantly affected by the absolute temperature.

## IV. Proposed Two-Quadrant Anti-Logarithmic Current Amplifier

This section focuses on the design of a two-quadrant current-mode ALOG amplifier circuit exhibiting temperature insensitivity. Fig. 6(a) depicts the fundamental building blocks for the proposed realization of a two-quadrant current-mode ALOG amplifier. Fig. 6(b) shows the practical realization derived from the principle depicted in Fig. 6(a) using the circuit functional blocks outlined in Section II.




(a)

(b)

Fig. 6. Proposed two-quadrant current-mode ALOG amplifier with temperature compensation.
(a) principle block diagram (b) transistor-level circuit

According to Fig. 6(b), the designed circuit was realized by applying the output currents $I_{o1}$ and $I_{o2}$ from Figs. 1 and 3, respectively, to the bias currents $I_1$ and $I_2$ of Fig. 2. This yields $I_1 = I_{o1} = |I_{in}|$ and $I_2 = I_{o2}$. Substituting $I_{o1}$ and $I_{o2}$ from (1) and (3) into (2), we obtain

$$I_4 = \left(\frac{V_T\,|I_{in}|}{I_3 R}\right)\ln\left(\frac{I_A}{I_B}\right) \quad . \tag{9}$$

The current $I_4$ now function as the bias current $I_D$ for the temperature-sensitive ALOG current amplifier $Q_{20}$-$Q_{22}$, where $I_D = I_4$. Consequently, the output current $I_{ALOG}$ of the proposed ALOG amplifier in Fig. 6(b) can be obtained by substituting $I_4$ from (9) into $I_D$ of (4), as given below:

$$I_{ALOG} = I_{o3} = I_C e^{\left(\frac{K_2 |I_{in}|}{I_3}\right)} \quad , \tag{10}$$

where

$$K_2 = \ln\left(\frac{I_A}{I_B}\right) \quad . \tag{11}$$

Equation (10) indicates that an anti-logarithmic function current generator can be constructed from Fig. 6(b). A salient characteristic to point out is that the circuit operates in two quadrants, controlled by only external bias currents, and is temperature independent.

## V. Consideration of Non-Ideal Performance

Ideally, we neglect the base current of the transistor and assume that all the transistors are identical. Nevertheless, in practice, low values of $\beta$ and a lack of transistor matching are significant factors that lead to errors in circuit performance. This effect could potentially appear in the current transfer characteristics of the proposed circuits, as discussed below.

Consider the absolute-value circuit $Q_1$-$Q_{10}$ in the proposed circuits of Figs. 5 and 6. If $\beta >> 1$, the base current of transistors can be neglected. However, in practice, the parameter $\beta$ has a finite value, which is, for example, equal to 80 for npn and 50 for pnp transistors. The current $I_{o1}$ can be contributed to a finite $\beta$. Therefore, the current $I_{o1}$ for both $I_{in}$ positive and negative signals can respectively be expressed in terms of $\beta$ as follows:

$$I_{o1} = \left(1 - \frac{2}{\beta_n^2 + 2\beta_n + 2}\right)\left(1 - \frac{2}{\beta_p^2 + 2\beta_p + 2}\right) I_{in} \cong \left(1 - \frac{2}{\beta_n^2}\right)\left(1 - \frac{2}{\beta_p^2}\right) I_{in}, \tag{12}$$

and

$$I_{o1} = \left(1 - \frac{1}{\beta_n^2 + 2\beta_n + 2}\right)\left(1 - \frac{2}{\beta_p^2 + 2\beta_p + 2}\right) I_{in} \cong \left(1 - \frac{1}{\beta_n^2}\right)\left(1 - \frac{2}{\beta_p^2}\right) I_{in}, \tag{13}$$

where $\beta_n$ and $\beta_p$ are the common-emitter current gains ($\beta$) of npn and pnp transistors, respectively. The only practical drawback with this circuit is the turning on and off of the transistors as $I_{in}$ alters polarity; consequently, $I_{o1}$ is not continuous when $I_{in}$ crosses zero. This can cause switching noise in the proposed circuit. Nevertheless, the circuit operates effectively, as will be demonstrated by the simulation results (Fig. 7) presented in the following section.

The non-ideal aspects of the current multiplier/divider circuit $Q_{11}$-$Q_{14}$ also affect the practicality of both proposed circuits. When the difference among the three currents ($I_1$, $I_2$, and $I_3$) is substantial, the effect of non-zero transistor base currents will be evident. For the temperature-dependent LOG current amplifiers $Q_{15A}$-$Q_{19A}$ and $Q_{15B}$-$Q_{19B}$ in Fig. 5, it is critical to set these three currents to guarantee a low discrepancy in magnitude. According to (3), in the ideal case, the output current $I_{o2}$ of the LOG current amplifier circuit is expected to be zero when $I_A/I_B$ equals unity. Nonetheless, non-zero base currents in bipolar transistors still induce a certain offset current at the output. The influence of this offset current on the proposed temperature-insensitive LOG amplifier circuit in Fig. 5 can be minimized by including a DC current source $I_{off}$ between +V and the output terminal (the collector terminal of $Q_{14}$) to get a zero-offset current, as depicted in Fig. 5.

In Fig. 6, the temperature-dependent ALOG amplifier in Fig. 4 performs the output section in the proposed ALOG current amplifier circuit with temperature compensation. If the ratio of $I_{ALOG}/I_C$ is of order $\beta^2$, then the base current of $Q_{21}$ becomes equivalent to $I_C$. Consequently, we cannot avoid the effect of the non-zero base current. The adjustment of $I_C$ is necessary to attain the designated emitter current value of $Q_{20}$. To overcome this problem, we could replace the bipolar transistor $Q_{21}$ with an NMOS transistor. The NMOS transistor will provide the bias current $I_D$, the base current of $Q_{22}$, and a suitable voltage to the base of $Q_{22}$ without influencing $I_C$ at any output current $I_{ALOG}$ level. Furthermore, inserting $I_{off}$ at the output terminal (the collector terminal of $Q_{22}$) may also enable the simple adjustment of the offset current, as illustrated in Fig. 6.

## VI. Functional Verification

PSPICE simulations have been carried out to demonstrate the versatility of the proposed LOG and ALOG amplifier circuits explained in Sections III and IV. The simulation has been performed using the mixed bipolar transistor array models of HFA3096 [14]. Both circuits were biased with a 2 V supply voltage and configured with $R = R_1 = R_2 = R_3 = 260\ \Omega$ for $V_T = 26$ mV at ambient temperature. To simplicity the design, the bias currents have been set at $I_A = 272\ \mu$A and $I_B = 100\ \mu$A, resulting in $K_1 = K_2 = 1$.

The simulation result of the absolute-value circuit in Fig. 5 demonstrates in Fig. 7 that the continuous transfer of current $I_{o1}$ is unfeasible when $I_{in}$ approaches zero. This primarily results from the activation and deactivation of the transistors, as previously discussed.

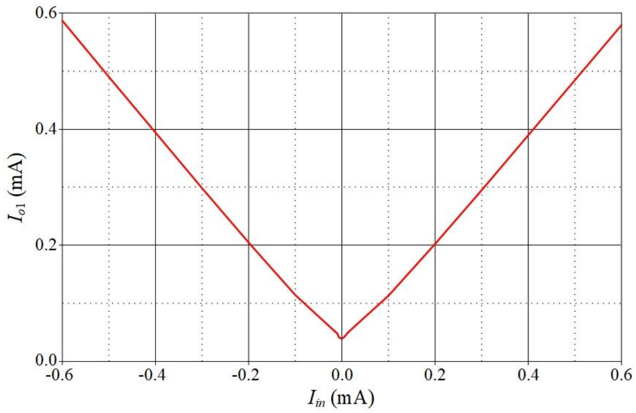



Fig. 7. Simulated DC current transfer characteristic of the absolute-value circuit.

Fig. 8 shows the ideal and simulated DC current transfer characteristic of the proposed two-quadrant current-mode LOG amplifier in Fig. 5 for the input current $I_{in}$, varying from -1 mA to 1 mA. As can be observed from Fig. 8, the resultant current characteristic is correctly related to the logarithmic function, corresponding well with the theoretical expectations. The results reveal a correct relationship between the resultant current characteristic and the logarithmic function, which aligns well with theoretical expectations.

In Fig. 9, the simulated output currents $I_{o2}$ and $I_{LOG}$ are shown in relation to the room temperature for the uncompensated and compensated temperature circuits depicted in Figs. 3 and 5, respectively. As can be observed, the temperature performance of the compensated circuit significantly surpasses that of the uncompensated circuit when the temperature is changed from -40°C to 100°C. Furthermore, as revealed in Fig. 9, the critical sensitivities of the output currents $I_{o2}$ and $I_{LOG}$ with respect to room temperature $T$ for both the uncompensated and compensated circuits, denoted as $S_T^{I_{o2}} = \frac{(\partial I_{o2}/I_{o2})}{(\partial T/T)}$ and $S_T^{I_{LOG}} = \frac{(\partial I_{LOG}/I_{LOG})}{(\partial T/T)}$, are roughly $318 \times 10^{-9}$ and $13.55 \times 10^{-9}$, respectively. Fig. 10 depicts the simulated AC current transfer characteristic of the proposed LOG current amplifier in Fig. 5, indicating that a practical frequency of around 20 MHz can be achieved.

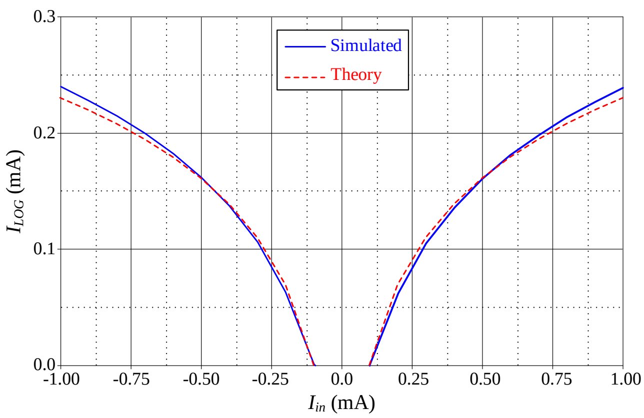



Fig. 8. DC current transfer characteristics of the proposed LOG current amplifier in Fig. 5.

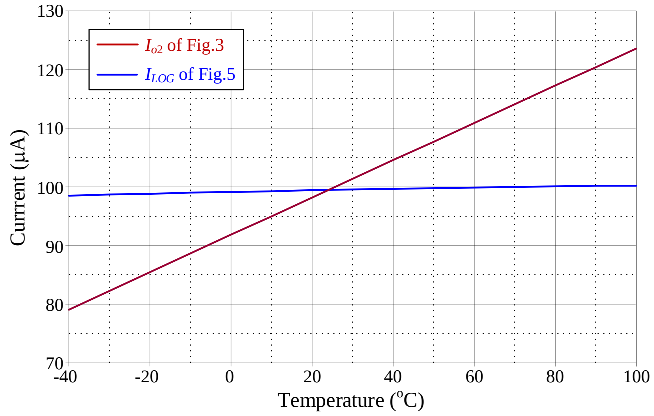



Fig. 9. Variations of the currents $I_{o2}$ and $I_{LOG}$ against room temperature.

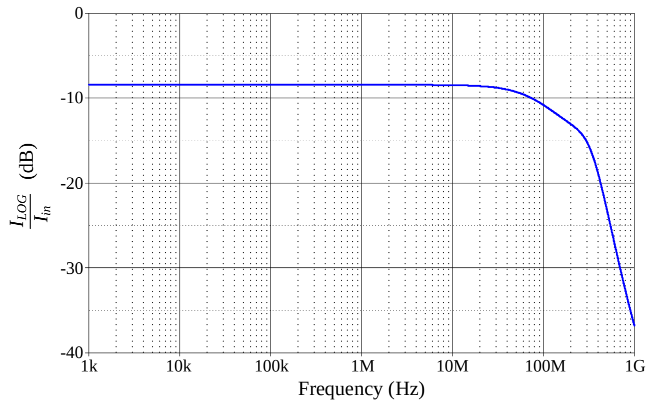



Fig. 10. Simulated AC current transfer characteristic of the proposed LOG current amplifier in Fig. 5.

Fig. 11 shows the ideal and simulated DC current transfer characteristic for the proposed ALOG current amplifier circuit depicted in Fig. 6. Fig. 12 illustrates the changes of the output currents $I_{O3}$ and $I_{ALOG}$ in relation of ambient temperature, corresponding to Figs. 4 and 6, respectively. The findings indicate that the relative sensitivities of $I_{O3}$ and $I_{ALOG}$ with respect to $T$ are obtained as $S_T^{I_{O3}} = \frac{(\partial I_{O3}/I_{O3})}{(\partial T/T)} = 72.75 \times 10^{-9}$ and $S_T^{I_{ALOG}} = \frac{(\partial I_{ALOG}/I_{ALOG})}{(\partial T/T)} = 1 \times 10^{-9}$, respectively. The suggested ALOG current function generator in Fig. 6 demonstrates significantly reduced temperature dependence, as desired. Additionally, Fig. 13 illustrates the frequency response simulation result, showing that the circuit functions up to approximately 20 MHz.

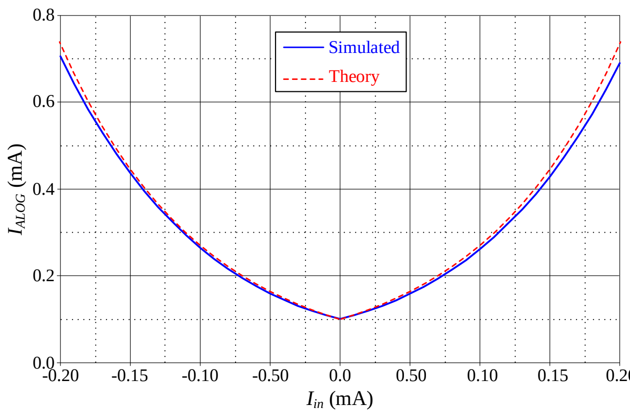



Fig. 11. DC current transfer characteristics of the proposed ALOG current amplifier in Fig. 6.

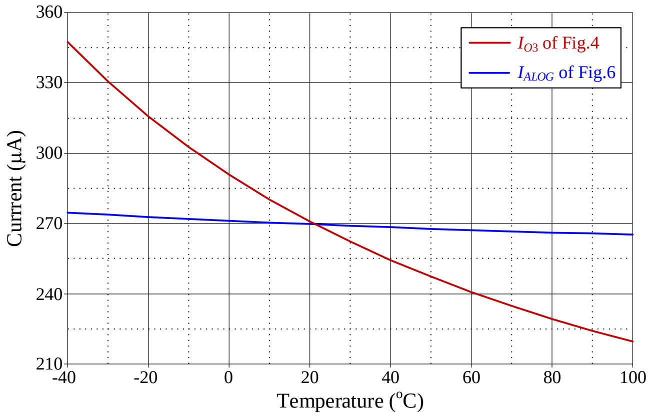



Fig. 12. Variations of the currents $I_{o3}$ and $I_{ALOG}$ against room temperature.

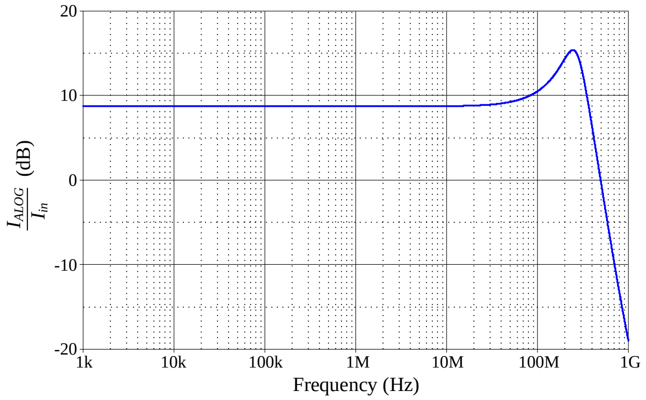



Fig. 13. Simulated AC current transfer characteristic of the proposed ALOG current amplifier in Fig. 6.

Finally, the simulation outcomes presented in Figs. 7-13 collectively confirm the expected behavior and robustness of the proposed two-quadrant LOG and ALOG amplifier circuits. Additonally, the frequency response plots of Figs. 10 and 13 show that both amplifiers support signal operation up to 20 MHz, confirming their suitability for high-speed analog processing. Despite minor discontinuities near zero input due to translinear switching in the absolute-value stage, the overall performance remains robust and predictable. These simulation findings validate the practicality and functional accuracy of the proposed designs under realistic conditions.

## VII. Conclusion

This work describes the circuit implementation of the two-quadrant logarithmic and anti-logarithmic function current generators that exhibit temperature insensitivity. The design is based on the current-mode translinear approach to generate the output currents that directly correspond to the absolute values of the logarithmic and anti-logarithmic functions. Both proposed circuits can operate in both positive and negative input current quadrants with a minimum supply voltage of 2V. A detailed analysis of the non-ideal performance of the proposed circuits has been discussed. PSPICE simulations in comparison to the theoretical results have been examined and validated the practical feasibility of the circuits. The simulation results demonstrate their excellent thermal stability.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